ADVANCE PROGRAM

2022 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY
20, 21, 22, 23, 24

CONFERENCE THEME:
Intelligent Silicon for a Sustainable World

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

DRAFT 11 - 18 - 2021

IEEE SOLID-STATE CIRCUITS SOCIETY

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: CX: Overcoming Data Bottleneck; Chip Design for Secure IoTs

12 TUTORIALS: Analog Circuits for BCD; High Frequency DC-DC Converters; Noise-Shaping SAR ADCs; Self-Sensing Processing Systems; Process Monitors for Signoff-Oriented Circuits; Power Transfer/Management for Medical Apps; HBM DRAM/3D Stacked; Mixed-mode RF Transceivers; Energy Harvesting Wireless Sensor Nodes; mm-Wave Phased-Arrays; Equalization Techniques; Digital vs. Analog AI Accelerators

2 EVENING EVENTS: Graduate Student Research in Progress; Next Gen Circuit Designer Workshop

THURSDAY ALL-DAY

4 FORUMS: Path to 6G; Paving the Way to 200Gb/s; Improve AI Efficiency; Computer Systems Under Attack

SHORT-COURSE: High Speed/High Performance Data Converters

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 20th, the day before the official opening of the Conference, ISSCC 2022 offers:

- A choice of 12 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums:

"Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing"

"Chip Design for Low-Power, Robust, and Secure IoT Devices"

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 20th, there are two events: "Next-Generation Circuit Designer 2022 Workshop" will be offered starting at 7:50 am. In addition, the Student-Research Preview, featuring ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 8:00 am. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community.

On Monday, February 21st, ISSCC 2022 at 8:30 am offers four plenary papers on the theme: "*Intelligent Silicon for a Sustainable World*". On Monday at 1:30 pm, there begin six parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. Monday evening includes two events, entitled, "*SemiConductor Supply Chain*" and "*Bright and Dark Side of AI*".

On Tuesday, February 22nd, there are six parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled "*Shifting Tides of Innovation*" and "*Next Trillion Dollar Market*".

On Wednesday, February 23rd, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 24th, ISSCC offers a choice of five all-day events:

- A Short Course entitled: "*High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics*"
- Four Advanced-Circuit-Design Forums entitled:

"The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing and Imaging"

"Paving the Way to 200Gb/s Transceivers"

"How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms"

"Computer Systems Under Attack – Paying the Performance Price for Protection"

This year, again, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course

Need Additional Information? Go to: www.isscc.org

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TUTORIALS

There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Naveen Verma
ISSCC Tutorials Chair

The presentations and the videos of all 12 tutorials (90 minutes each)
will be available online, on-demand, as of:
Friday, Feb. 11, 2022, 5:00pm, EST

Live Q&A sessions for the tutorials will be available on:
Sunday Feb. 20, 2022, 9:00am - 11:00am EST

20 minute live session = 5 minute summary + 10 minute Q&A + 5 minute break

The Q&A sessions will be recorded and made available after their live sessions.

Live Q&A - February 20, 9:00am EST

T1: Analog Circuit Design in Bipolar-CMOS-DMOS (BCD) Technologies

Marco Berkhout, *Goodix Technology, Nijmegen, The Netherlands*

Biopolar-CMOS-DMOS (BCD) technologies enable applications of high industrial interest, whereby high-voltage and high-power circuits are combined with high-density digital logic on a single die, as in (audio) power amplifiers and switch-mode power supplies (SMPS). This tutorial addresses challenges of BCD design that are not usually encountered when designing in standard CMOS, e.g. crossing (multiple) voltage domains, parasitic bipolar activity with inductive loads, large operating supply voltage ranges and electrostatic discharge (ESD). The tutorial looks into the structure of BCD technologies and devices, as well as typical circuits, such as power switches, gate drivers, level shifters and bootstraps.

Marco Berkhout received the M.Sc. and the Ph.D. degrees in EE from the University of Twente, The Netherlands, in 1992 and 1996. From 1996 to 2019, he was with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He is currently a fellow with Goodix Technologies, Nijmegen. His main interests are class-D amplifiers and integrated power electronics. Dr. Berkhout was a TPC member of the European Solid-State Circuits Conference (ESSCIRC) from 2008 to 2018 and the International Solid-State Circuits Conference (ISSCC) from 2013 to 2016, and since 2021. He received the ESSCIRC 2002 Best Paper Award and was a plenary invited speaker at the ESSCIRC 2008.

Live Q&A - February 20, 9:00am EST

T2: Fundamentals of High-Frequency DC-DC Converters

Kousuke Miyaji, *Shinshu University, Nagano, Japan*

Advances in CMOS processes and the spread of GaN FETs are pushing the switching frequency of DC-DC converters beyond 10MHz. Such increase in the switching frequency of the conveters results in reducing the size of passive components and increasing the system power density. Starting from the fundamentals of DC-DC buck converters, this tutorial will cover topics including loss analysis and control schemes at high frequencies typically above a few MHz. State-of-the-art design techniques to reduce the switching loss and to drive GaN FETs are also introduced. Finally, topics including recent progress in high-frequency magnetic components and their integration will be covered.

Kousuke Miyaji received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2003, 2005, and 2008, respectively. He is currently an Associate Professor in the Department of Electrical and Computer Engineering at Shinshu University. His current research interests include high-frequency DC-DC converters, efficient power-management systems, wireless power transfer systems, and 3D-integration of power magnetic components. Dr. Miyaji has been serving as a TPC member of the International Solid-State Circuits Conference (ISSCC) since 2021.

Live Q&A - February 20, 9:00am EST

T3: Noise-Shaping SAR ADCs

Yun-Shiang Shu, *MediaTek, Hsinchu City, Taiwan*

The noise-shaping (NS) successive-approximation register (SAR) has become a dominant emerging ADC architecture in a short time. Combining the benefits of SAR and noise shaping, NS-SAR ADCs take full advantage of advanced CMOS processes and continue to break records for energy and area efficiency. Along with increasing data rate, NS-SAR ADCs are getting attractive in various applications. This tutorial begins by explaining the basics of the NS SAR. It explores different noise-shaping techniques and introduces approaches for higher-order noise-shaping and high signal-bandwidth designs.

Yun-Shiang Shu (S'05–M'10–SM'19) received the B.S. and M.S. degrees in Electrical Engineering from National Taiwan University, Taiwan, in 1997 and 1999, respectively, and the Ph.D. degree in electrical and computer engineering from University of California at San Diego, CA in 2008. He is currently a Deputy Technical Director at MediaTek Inc., Hsinchu, Taiwan, where he leads the development of biosensors for wearable devices. His published works in ISSCC, VLSI, and JSSC range from flash, pipeline, SAR, to delta-sigma ADCs for communication and sensor interface applications, with a focus on signal processing techniques to compensate for analog circuit imperfections. Dr. Shu was a TPC member of the IEEE Symposium on VLSI Circuits and currently serves as an ITPC member and Far-East Regional Chair for IEEE ISSCC 2022.

Live Q&A - February 20, 9:00am EST

T4: Fundamentals of Self-Sensing Processing Systems

Shidhartha Das, *Arm, Cambridge, United Kingdom*

High-performance systems are challenged by the stringent computational, reliability and availability requirements of emerging cloud-native applications. Unfortunately, efficiency gains through scaling alone have slowed, even as susceptibility to variation-induced system failures have increased, thus necessitating further innovations in energy efficient and reliable processor and system design. This tutorial addresses the following key aspects: how do sources of variations impact design margins and system reliability?; how do self-monitoring systems use sensors to measure ambient environment?; how is environment adaptation actuated in high-volume production systems using a combination of power-delivery and clocking techniques?; what design and analysis techniques can mitigate transient soft errors and hard errors due to transistor aging and interconnect failures?

Shidhartha Das received the M.Sc. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 2003 and 2009, respectively. He is currently a Distinguished Engineer with Arm Ltd., Cambridge, UK where he conducts research in high-performance CPU design, focusing on circuit/micro-architectural techniques for power delivery and variation mitigation. In the past, he has contributed to multiple areas of technology development, including mixed-signal architectures for machine-learning acceleration and emerging non-volatile memories, for which he received the Arm Inventor of the Year award in 2016. He has 58 granted US patents and several more that are pending. He has received multiple best paper awards and his research has been featured in IEEE Spectrum. He serves as the Guest Editor for the IEEE Journal of Solid-State Circuits and Associate Editor for the IEEE Solid-State Circuits Letters.

Live Q&A - February 20, 9:00am EST

T5: Fundamentals of Process Monitors for Signoff-Oriented Circuit Design

Eric Jia-Wei Fang, *Mediatek, Hsinchu City, Taiwan*

In advanced technology nodes, the process technology requires more than a year to reach maturity. To avoid costly iterations between design and foundry, thus impeding time-to-market, the final validation of circuit timing and power, known as chip signoff, should leverage on-chip process monitors to speed-up process learning. This tutorial introduces the relationship between process and signoff in terms of speed/leakage, voltage, temperature and aging. Then, the tutorial covers the different types of digital circuits, with a focus on the corresponding challenges, to monitor this relationship. Since signoff requires a statistical methodology, silicon big-data collection and analysis are described to provide feedback to the foundry and designers.

Eric J.-W. Fang received the B.S. degree in electrical engineering from National Cheng Kung University, Taiwan in 2003, and the M.S. and Ph.D. degrees in electronics engineering from National Taiwan University, Taiwan in 2005 and 2009, respectively. He was a Visiting Scholar with the University of Illinois at Urbana-Champaign, Champaign, USA between 2008 and 2009. He is currently a senior department manager with MediaTek, Inc. and has served as an International Technical Program Committee member for IEEE ISSCC since 2021. His current research interests include digital sensor design with machine-learning technology, digital timing and IR signoff, and chip-package-board co-design. He has published more than 15 technical papers and holds 10 granted US patents.

Live Q&A - February 20, 9:00am EST

T6: Wireless Power Transfer and Management for Medical Applications

Mehdi Kiani, *The Pennsylvania State University, University Park, PA*

Wireless technologies play an important role in advanced biomedical systems. Implantable medical devices (IMDs) are a rapidly growing category of bio-systems, where the use of wireless technology is a necessity. This tutorial will present several system- and circuit-level techniques towards the development of novel wireless power-transfer systems with different modalities. Also, novel integrated power-management circuits with voltage and current mode operation will be reviewed.

Mehdi Kiani received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from the Georgia Institute of Technology in 2012 and 2013, respectively. He joined the faculty of the School of Electrical Engineering and Computer Science at the Pennsylvania State University in August 2014 where he is currently an Associate Professor. His research interests are in the multidisciplinary areas of analog, mixed-signal, and power-management integrated circuits, wireless implantable medical devices, neural interfaces, and assistive technologies. He was a recipient of the 2020 NSF CAREER Award. He is currently an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems and IEEE Transactions on Biomedical Engineering.

Live Q&A - February 20, 10:00am EST

T7: HBM DRAM and 3D Stacked Memory

Dong Uk Lee, *SK hynix, Icheon-si, Korea*

The proliferation of machine-learning workloads has accelerated the demand for higher memory bandwidth in modern systems. HBM DRAM was developed to break through the system-performance limit caused by memory bandwidth. With advanced packaging technology, HBM has been the only scalable DRAM bandwidth solution of the past 10 years, starting from 128GB/s and now extending beyond 800GB/s. This tutorial will cover HBM, HBM2, and HBM3 architectures; it will also cover historical trends and state-of-the-art of DRAM. Electrical interfaces and PDN for 2.5D system-in-package (SiP) structures will be reviewed, along with heterogeneous memory structures, including TSV interfaces. This tutorial will also cover the various design methods such as known-good-stack verification, self-repair, MBIST and RAS features, to deal with the new package structures. Finally, advanced 3D memory architectures including future trends of HBM, will be introduced.

Dong Uk Lee is Principal Engineer of SK hynix. He was the Lead Engineer of the industry's first HBM DRAM development and standardization from 2011 to 2013. He received the B.S. and M.S. degrees in electronics from Hanyang University, Seoul, Korea, in 1996 and 2001. He joined Hynix in 2001, and has developed 16 commodity DRAMs, including graphics DRAM, computing DRAM, HBM, HBM2E and HBM3. He holds 70 US patents. He is the author of 8 ISSCC and 2 JSSC, from 2006 to 2020. He presented an invited paper at CICC 2015, and he was a forum presenter at ISSCC 2016. Mr. Lee received the Medal of Honor for outstanding contribution to the semiconductor industry from the Government of Korea in 2021. Since 2017, he has been serving as a member of the ISSCC Technical Program Committee.

Live Q&A - February 20, 10:00am EST

T8: Fundamentals of Mixed-Mode RF Transceivers

Jeff Walling, *Virginia Tech, Blacksburg, VA*

RF systems that directly interface between digital bits and RF front-ends are rapidly gaining interest as the number of transceivers in mobile systems is increasing. This tutorial will review the concepts of direct digital-to-RF conversion and focus on the analysis and design of digital transceiver building blocks, such as switched capacitor RF-DACs, current-mode RF-DACs, and directly quantized receiver circuits. The tutorial will focus on the practical implementation of these circuit blocks using theoretical predictions.

Jeff Walling received his PhD degree from the University of Washington in 2008 and has been actively engaged in research and product design in the wireless industry for 20 years. While a student and intern at Intel Research, he was an early pioneer in digital friendly and mixed-mode transceiver systems and has continued to lead innovation in the field, particularly with the introduction of the switched-capacitor power amplifier. He has published >70 journal and conference papers and has twice won outstanding department teaching awards at Rutgers University and the University of Utah. He was in the corporate R&D group at Qualcomm and the AI solutions sector at Skyworks. Since the Fall of 2021, he is an Associate Professor in the ECE department at Virginia Tech. His research is focused on efficient radio architectures from RF-to-THz for next generation communication networks.

Live Q&A - February 20, 10:00am EST

T9: Design Methodologies for Energy Harvesting Wireless Sensor Nodes

Sriram Vangal, *Intel, Hillsboro, OR*

Wireless sensor nodes (WSNs) for IoT systems need to enable always-on always-sensing (AOAS) and advanced edge-computing capabilities under stringent energy constraints, often supported mainly by harvested energy. After an introduction into WSNs and their implementation challenges, this tutorial provides an overview of key blocks, designs, and system-level optimizations to enable energy-efficient WSN silicon. Multi-layered co-optimization approaches that crosscut architecture, devices, near-threshold voltage (NTV) logic and SRAM circuits, NTV cell libraries, low-power tool flows/methodologies, and aggressive power management techniques are required for realizing energy-efficient (μW) WSNs. The tutorial will also cover emerging trends in embedded energy-harvesting circuits, necessary to work in harmony with smart and fine-grain power management of different components of the WSN for realizing secure, AOAS-capable energy-neutral WSN systems.

Sriram Vangal received the B.E. degree from Bangalore University, India, in 1993, the M.S. degree from the University of Nebraska, Lincoln, USA in 1995, and the Ph.D. degree from Linköping University, Sweden in 2007 – all in Electrical Engineering. He joined Intel Corporation in 1995 and has played a lead role in multi-core CPU development and ultra-low power silicon research. Sriram is a Principal Engineer with Intel Labs researching sustainable net-zero energy computing. Sriram has received two Intel Achievement Awards for his work, is an IEEE senior member and has published over 35 conference and journal papers, has authored three book chapters, and has over 30 issued patents.

Live Q&A - February 20, 10:00am EST

T10: Fundamentals of mm-Wave Phased-Arrays

Bodhisatwa Sadhu, *IBM T. J. Watson Research Center, Yorktown Heights, NY*

Millimeter(mm)-Wave phased arrays are becoming a differentiating technology in modern wireless communication and imaging systems. This tutorial will cover key aspects of silicon-based mm-wave phased-array IC design and package integration. It will begin with an overview of the theory and intuition behind phased arrays; it will then discuss different silicon-based phased-array architectures and key phased-array building blocks, including phase shifters, variable-gain amplifiers, combiners, and splitters. Finally, this tutorial will discuss the integration of phased-array ICs with antennas in phased-array antenna modules.

Bodhisatwa Sadhu received the B.E. degree in electrical and electronics engineering from Birla Institute of Technology and Science (BITS) – Pilani, India in 2007, and the Ph.D. degree in Electrical Engineering from the University of Minnesota, Minneapolis, in 2012. He is currently a Research Scientist at IBM T. J. Watson Research Center, NY, and an Adjunct Assistant Professor at Columbia University, NY. At IBM, he led the design of the world's first reported silicon-based 5G phased array IC. He has authored/co-authored 50+ papers, a book, and several book chapters, and holds 50+ issued U.S. patents. He is the recipient of multiple awards including the 2017 ISSCC Lewis Winner Award for Outstanding Paper and the 2017 JSSC Best Paper Award. He is an MTT-S Distinguished Microwave Lecturer, and serves on the steering committee of IEEE RFIC Symposium, and the ITPC of IEEE ISSCC.

Live Q&A - February 20, 10:00am EST

T11: Basics of Equalization Techniques: Channels, Equalization, and Circuits

Byungsub Kim, *Pohang University of Science and Technology, Pohang, Korea*

This tutorial presents basic equalization techniques for high-speed serial interfaces. A simple channel transfer function model will be discussed to explain various channel behaviors. Basic transmitter and receiver equalization techniques such as feed-forward equalization (FFE), continuous-time linear equalization (CTLE), and decision-feedback equalization (DFE) will be covered. Modulation techniques such as non-return-to-zero (NRZ), duo-binary, and pulse-amplitude modulation 4 (PAM-4) will be discussed. Various implementations and design challenges of equalization circuits will be discussed and compared. Various methods of equalization adaptation algorithms will be covered.

Byungsub Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively. He was an Analog Design Engineer with Intel Corporation, Hillsboro, OR, USA, from 2010 to 2011. In 2012, he joined the Faculty of Department of Electrical Engineering, POSTECH, where he is currently an Associate Professor. Dr. Kim received several honorable awards. He was a recipient of the IEEE Journal of Solid-State Circuits Best Paper Award in 2009. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE Internal Solid-State Circuits Conference. He has been serving as a Technical Program Committee Member of IEEE International Solid-State Circuits Conference since 2018.

Live Q&A - February 20, 10:00am EST

T12: Advances in Digital vs. Analog AI Accelerators

Jae-sun Seo, *Arizona State University, Tempe, AZ*

For state-of-the-art AI accelerators, there have been large advances in both all-digital and analog/mixed-signal circuit-based designs. This tutorial presents a practical overview and comparison of recent digital and analog AI accelerators. It will first introduce recent AI algorithms for computer vision and speech applications, which have been targeted for many AI hardware designs. Next, it will present a survey of (i) all-digital AI accelerators, including designs with new dataflow, low precision, and sparsity, and (ii) analog/mixed-signal AI accelerators featuring switch-capacitor circuits and in-memory computing with analog-to-digital converters. The tutorial discusses the key trade-offs of both design approaches including circuit/architecture design, algorithm-mapping flexibility, hardware accuracy and energy efficiency.

Jae-sun Seo received the Ph.D. degree from the University of Michigan in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center. In 2014, he joined ASU in the School of Electrical, Computer and Energy Engineering, where he is now an Associate Professor. He was a visiting faculty at Intel Circuits Research Lab in 2015. His research interests include efficient hardware design of machine learning and neuromorphic algorithms. He has authored/co-authored >130 papers and holds >10 issued U.S. patents. He is a recipient of an IBM Outstanding Technical Achievement Award (2012), an NSF CAREER Award (2017), and an Intel Outstanding Researcher Award (2021). He currently serves as an International Technical Program Committee member for ISSCC and an Associate Editor for IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS).

F1: Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing

Organizer: ***Kyu-Hyoun (KH) Kim,*** *IBM T. J. Watson, Yorktown Heights, NY*

Committee: ***Geoffrey W. Burr,*** *IBM Research, San Jose, CA*
Jun Deguchi, *Kioxia, Kawasaki, Japan*
Eric Wang, *TSMC, Hsinchu, Taiwan*
Chih-Cheng Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*

Champions: ***Yan Li,*** *Western Digital, Milpitas, CA*
Fatih Hamzaoglu, *Intel, Hillsboro, OR*

As AI network- and dataset-sizes keep growing, the flow of data – from various tiers of the memory hierarchy to the compute-engines, and back – becomes critically important. In the worst-case, this data-flow can start to constrain further improvements in both system-performance and the energy-efficiency of future AI processing systems.

The idea of processing data at the spot where it is stored or generated, instead of moving it back and forth, has led to a broad variety of promising compute-in-x system concepts; where, x can be a memory array, a memory die, a memory package, the storage, a sensor, the network, etc.

This forum will highlight the state-of-the-art for several such compute-in-x system concepts, as well as related in-the-near-future challenges and opportunities for the SSCS community.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Kyu-Hyoun (KH) Kim,*** *IBM T. J. Watson, Yorktown Heights, NY*
8:20 AM	**AI Memory Challenges and How to Solve Them For Data-Flow Accelerators** ***Swagath Venkataramani*****,** *IBM T. J. Watson, Yorktown Heights, NY*
9:05 AM	**Nano-Systems for AI:** ***N3XT 3D*** **with Dense-Memory, Illusion-Scaleup, Co-Design** ***Subhasish Mitra*****,** *Stanford University, Stanford, CA*
9:50 AM	Break
10:00 AM	**Computing In and Near Memory: Practical Challenges and Future Directions** ***Nam Sung Kim*****,** *University of Illinois, Urbana, IL*
10:45 AM	**Future Prospects of Computing In or Near Flash Memories** ***Hang-Ting (Oliver) Lue*****,** *Macronix International, Hsinchu, Taiwan*
11:30 AM	**We've Rethought Our Commute; Can We Rethink Our Data's Commute?** ***Frank Hady*****,** *Intel, Portland, OR*
12:15 PM	Lunch
1:30 PM	**6G: Convergence of Communication, Computing, Control and Sensing** ***Mallik Tatipamula*****,** *Ericsson, Santa Clara, CA*
2:15 PM	**Charge-Domain Signal Compression in Ultra-High-Speed CMOS Image Sensors** ***Keiichiro Kagawa*****,** *Shizuoka University, Hamamatsu, Japan*
3:00 PM	Break
3:15 PM	**Neuromorphic Computing** ***Steve B. Furber*****,** *The University of Manchester, Manchester, United Kingdom*
4:00 PM	Conclusion

F2: Chip Design for Low-Power, Robust, and Secure IoT Devices

Organizer: ***Patrick Mercier,*** *University of California, San Diego, CA*

Committee: ***Rabia Tugce Yazicigil*****,** *Boston University, Boston, MA*
Jan Prummel**,** *Dialog Semiconductor B.V., A Renesas Company, 's-Hertogenbosch, The Netherlands*
Luca Benini**,** *ETHZ and UNIBO, Zurich, Switzerland*
Gael Pillonnet**,** *CEA-Léti, Grenoble, France*
Hidehiro Shiga**,** *KIOXIA, Yokohama, Japan*

Champions: ***Yun-Shiang Shu,*** *MediaTek, Taipei, Taiwan*
Andreia Cathelin, *STMicroelectronics, Crolles, France*
Bruce Rae, *STMicroelectronics, Edinburgh, United Kingdom*

The Internet of Things is currently in the process of transitioning from concept to execution, and yet, many technical challenges remain. In particular, emerging IoT devices require increasingly small form factors and therefore must consume very low power, all while operating in congested wireless environments with security designed-in from the ground up. Emerging devices also require built-in machine-learning capabilities in tiny footprints while consuming low power.

This forum covers topics ranging from how to build energy-efficient yet long-range and robust IoT-centric wireless links, how to build low-power sensor interfaces, how to design physically and cryptographically-secure protocols, how to integrate signal processing and machine learning into small nodes, and how to perform efficient yet compact power management/energy harvesting.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Patrick Mercier,*** *University of California, San Diego, CA*
8:20 AM	**Connecting Massive IoT in the New Decade and Beyond** ***Tingfan Ji*****,** *Qualcomm, San Diego, CA*
9:05 AM	**Sensor Interface, Analog, and Mixed-Signal Circuits for Miniaturized IoT Devices** ***Taekwang Jang*****,** *ETH Zurich, Zurich, Switzerland*
9:50 AM	Break
10:00 AM	**Wide-Range Wireless Communication Circuits for NB-IoT and eMTC** ***Kim B. Östman*****,** *Nordic Semiconductor, Turku, Finland*
10:45 AM	**Low-Power Wireless Communication Technologies for Emerging Short-Range Internet-of-Things** ***Po-Han Peter Wang*****,** *Broadcom, San Diego, CA*
11:30 AM	**Manufacturing Semiconductors is Complex. How About Manufacturing Secure Semiconductors?** ***Miroslav Knezevic*****,** *NXP, Austin, TX*
12:15 PM	Lunch
1:30 PM	**Memory System Design to Innovate Edge Computing for IoT Devices** ***Takashi Ito*****,** *Renesas Electronics, Tokyo, Japan*
2:15 PM	**Energy-Constrained Tiny-ML for IoT Applications** ***Tony Tae-Hyoung Kim*****,** *Nanyang Technological University, Singapore, Singapore*
3:00 PM	Break
3:15 PM	**Extending Battery Life Through Lower I_Q without Compromising System Performance or Solution Size** ***Keith Kunz,*** *Texas Instruments, Tucson, AZ*
4:00 PM	Conclusion

SE1: Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 90 second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in two theme sections: Digital and Machine-Learning; Analog and Radio.

The Student Research Preview will include a Distinguished Lecture by Prof. Kofi Makinwa, Delft University of Technology. SRP is open to all ISSCC registrants.

SRP Session (8:00 AM – 10:00 AM)

8:00 AM:	**Introductory Remarks**
8:05 AM:	**Awards** Silk Road Award SSCS Pre-Doctoral Fellowship Award ISSCC Student Travel Grant
8:15 AM:	**Distinguished Speaker Talk** *(pre-recorded, streamed live)* ***"First Tme Right!"*** by Prof. Kofi Makinwa, Delft University of Technology
8:30 AM - 9:00 AM:	**90 Second Presentations** *(pre-recorded, streamed live)*
9:00 AM - 10:00 AM:	**Posters** *(Gathertown, live)*

Evening Meet-The-Mentor Session (8:00 PM – 10 PM)

SRP Organizing Committee

Co-Chair:	**Jerald Yoo**	National University of Singapore, Singapore
Co-Chair:	**Mondira Pant,**	Intel, MA
Advisor:	**Anantha Chandrakasan**	MIT
Advisor:	**Kevin Zhang**	TSMC
Advisor:	**Jan Van der Spiegel**	University of Pennsylvania
Media/Publications:	**Laura Fujino**	University of Toronto
A/V:	**Trudy Stetzler**	Halliburton, Houston, TX

Committee Members

Masoud Babaie, Delft University of Technology, Netherlands

Utsav Banerjee, Indian Institute of Science, India

Hsin-Shu Chen, National Taiwan University, Taiwan

Po-Hung Chen, National Chiao Tung University, Taiwan

Zeynep Deniz, IBM, NY

Hao Gao, Eindhoven University of Technology, Netherlands

Minkyu Je, KAIST, Korea

Matthias Kuhl, Hamburg University of Technology, Germany

Seulki Lee, IMEC-NL, Netherlands

Yoonmyung Lee, SungKyunKwan University, Korea

Shih-Chii Liu, University of Zurich/ETH Zurich, Switzerland

Carolina Mora Lopez, imec, Belgium

Noriyuki Miura, Osaka University, Japan

Phillip Nadeau, Analog Devices, MA

Mondira Pant, Intel, MA

Negar Reiskarimian, MIT, MA

Jae-sun Seo, Arizona State University, AZ

Atsushi Shirane, Tokyo Institute of Technology, Japan

Mahsa Shoaran, EPFL, Switzerland

Yildiz Sinangil, Apple, CA

Mahmut Sinangil, TSMC, CA

Filip Tavernier, KU Leuven, Belgium

Chia-Hsiang Yang, National Taiwan University, Taiwan

Lita Yang, Microsoft, CA

Rabia Tugce Yazicigil, Boston University, MA

Jerald Yoo, National University of Singapore, Singapore

Milin Zhang, Tsinghua University, China

SE2:
Morning Session: Next Generation Circuit Designer 2022 Workshop

Chair: Yildiz Sinangil, *Apple, Cupertino, CA*
Co-Chair: Sophia Shao, *UC Berkeley, Berkeley, CA*
Co-Chair: Alice Wang, *Everactive, Plano, TX*

Workshop Committee:

Abira Alvater, IEEE-SSCS, New Jersey
Aya G. Amer, MIT, Cambridge, MA
Zeynep Deniz, IBM
Najme Ebrahimi, University of Florida, Gainesville, FL
Dina Reda El-Damak, University of Science and Technology at Zewail City, Egypt
Yasemin Engur, Middle East Technical University, Turkey
Q. Jane Gu, University of California Davis, CA
Ulkuhan Guler, Worcester Polytechnic Institute
Yaoyao Jia, University of Austin, Texas
Awani Khodkumbhe, Texas Instruments, India
Rabia Yazicigil Kirby, Boston University, Boston, MA
Alicia Klinefelter, NVIDIA, Santa Clara, CA
Deeksha Lal, Anokiwave, Billerica, MA
Jiamin Li, National University of Singapore, Singapore
Rikky Muller, University of California, Berkeley, CA
Farhana Sheikh, Intel, Hillsboro, OR
Trudy Stetzler, Halliburton, Houston, TX
Vivienne Sze, Cambridge, MA
Kathy Wilcox, AMD

Advisory Board:

Anantha Chandrakasan, *MIT, Cambridge, MA*

The IEEE SSCS Women in Circuits together with ISSCC will be co-sponsoring the first "Next Generation Circuit Designer 2022" for young professionals and students. This is a virtual educational workshop for a diverse set of graduate and undergraduate students, and young professionals who have graduated with B.S. within the last two years, who are interested in learning how to excel at academic and industry careers in computer science and computer and electrical engineering.

The panel on "Our Path to Circuit Design", with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

In addition to the panel, we will be selecting forty next generation circuit designers in academia and industry to attend a keynote from a distinguished speaker, an informal fireside chat with a high-profile leader in the field, and participate in an elevator pitch. The selected designers will also get the opportunity for networking and mentoring through virtual events leading up to the workshop. The morning virtual event will be followed by an optional evening in-person event, which will include further networking opportunities.

SE2:
IEEE SSCS WiC Rising Stars 2020 Workshop Schedule

7:50AM – 8:15AM: **Welcome, Video by Rising Stars 2020**

8:00AM – 8:10AM: **Workshop Opening and Introduction**
Yildiz Sinangil, *Apple, Cupertino, CA*
Alice Wang, *Everactive, Plano, TX*
Sophia Shao, *University of Berkeley, Berkeley, CA*

7:50AM – 8:15AM: **Video by Rising Stars, presented by Kathy Wilcox**

8:15AM – 9:00AM: **Fireside Discussion with**
Megan Smith, *United States Chief Technology Officier (CTO) of the United States*

Introduction and Facilitator:
Rabia Yazicigil, *Boston University, Boston, MA*

9:05AM – 10:00AM: **Next Generation Circuit Designers Elevator Pitch**

Introduction and Facilitator:
Najme Ebrahimi, *University of Florida, Gainesville, FL*
Deeksha Lal, *Anokiwave, Billerica, MA*

Forty selected next generation circuit designers will have the chance to give an elevator pitch to the attendees.

10:05AM – 10:45AM: **Special Talk by Tsu-Jae King Liu,** *University of Berkeley, CA*

Introduction and Facilitator:
Alicia Klinefelter, *NVIDIA, Durham, NC*

10:50AM – 11:50AM: **Our Path To Circuit Design Panel**

Panel Moderator:
Dina Reda El-Damak, *University of Science and Technology at Zewail City, Egypt*

The panel on "Our Path to Circuit Design", with panelists from diverse regions, backgrounds and career levels, will touch upon topics such as:

- networking and mentoring,
- choosing or changing a career path, a research topic, or an advisor,
- time management, work-life balance, and mental and physical well-being,
- managing day-to-day life in both graduate school and industry,
- dealing with challenges and conflict, and more.

Panelists:
Alvin Loke, *NXP, San Jose, CA*
Andreia Cathelin, *ST Microelectronics, Grenoble, France*
Canan Dagdeviren, *MIT, Cambridge, MA*
Ada Poon, *Stanford University, Stanford, CA*
Brian Floyd, *North Carolina State University, Raleigh, NC*

Plenary Session — Invited Papers

Session Chair:
Kevin Zhang, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
ISSCC Conference Chair

Session Co-Chair:
Edith Beigné, *Meta, Menlo Park, CA*
ISSCC International Technical Program Chair

8:30 AM
FORMAL OPENING OF THE CONFERENCE

8:45 AM

1.1 Catalysts of the Impossible: Silicon, Software, and Smarts for the Era of SysMoore

Aart de Geus, *Chairman & Co-CEO, Synopsys, Mountain View, CA*

As we confront global scale challenges with immense intertwined datasets, the distillation of usable insights will require an exponential increase in AI processing capability. The impossibility horizon – sustained by the slowing of Moore's Law – will be pierced by rapid advancements in materials, devices, software, and architecture (the '*SysMoore*' era).Autonomous design *instruments* – super-tools fusing together hundreds of algorithms precision-guided by AI – are unlocking opportunity for circuit designers ushering in a new wave of architectural vitality.

In the follow up to '*Builders of the Imaginary*', we will unveil the next chapter in autonomous design, piecing together a new breed of super-monolithic devices, dense interconnects, and chiplets, into software-defined, heterogeneous architectures.

9:20 AM

1.2 The Future of the High-Performance Semiconductor Industry and Design

Renée James, *Founder, Chairman, & CEO, Ampere Computing, Santa Clara, CA*

While the explosive growth of today's modern cloud was fueled by high performance, present- day efficient modern cloud services have moved to a new phase of compute that require scalability and elasticity, while still achieving the highest performance levels to run a myriad of cloud services. The new breed of software underlying today's cloud services is initiating a third phase of compute unencumbered by architectural complexity designed for client- and server-enterprise applications. Initially, cloud computing was able to leverage traditional processor architectures to deliver value to the end customers. However, massive adoption of cloud-based services has amplified the limitations of the incumbent architectures that were designed for a very different software model in client-server enterprises. The requirement of high-performance for cloud computing has fundamentally changed from one of peak performance at a CPU-level to overall performance at the system-level. This system-level performance refers to maximizing system-level throughput while staying within or further reducing power and cost envelopes, and with much higher emphasis on predictable and consistent performance. This cloud-driven computing requires a fundamental shift in the processor, as well as in SOC architectures and designs, and demands continued innovation to stay ahead of cloud computing growth for the next decade. These innovations need to address the entire vertical stack from software, architecture, design, to packaging and manufacturing domains. The paper will discuss a new approach in architectural thinking and design based on cloud computing as the driving force for demand.

9:55 AM

ISSCC, SSCS, IEEE Award Presentations

10:20 AM

Break

10:40 AM

1.3 Intelligent Sensing: Enabling the Next "Automation Age"

Marco Cassis, *President, Sales, Marketing, Communications & Strategy Development*
STMicroelectronics, Geneva, Switzerland / Tokyo, Japan

Sensors have undergone extraordinary proliferation since the beginning of the 21st Century. Thanks to IoT, connected smart sensors can now be found all around us. This makes it possible to collect a wealth of data autonomously and continuously without human intervention, automating routine activities while unlocking previously unattainable insights and functionality. As we enter the Automation Age, the information generated from these sensors can be processed and acted on locally to take action in the physical world.

Sensing, artificial intelligence, and actuation will enable autonomous end-to-end system solutions in existing and new application fields including automotive, digital health, agriculture, environmental control, and decarbonization. The Semiconductor Industry is driving this transformation and sensors, smart embedded actuators, analog interfaces, connectivity, security and embedded AI, offer a perfect toolset for companies to continue to innovate. To fuel this innovation, we need to develop energy-efficient, high-accuracy, autonomous, ultra-compact, and trusted ICs. These chips need to feature state-of-the-art system and embedded security techniques to protect the gathered data, its processing and the resulting actuation. New and super-efficient computational hardware technologies supporting AI and machine learning are already transforming at-the-edge data processing and are pushing the envelope on intelligent functionality and IoT network scalability.

Future advances will rely on these evolving IC technologies as well as associated packaging solutions. These will include super-integration, wafer-to-wafer bonding, and system-in-package, to enable the heterogenous integration of multiple technologies.

11:15 AM

1.4 The Art of Scaling: Distributed and Connected to Sustain the Golden Age of Computation

Inyup Kang, *President, Samsung Electronics, Hwaseong, Korea*

The history of the computer has been nothing but miraculous! Thanks to the rapid innovations in semiconductor manufacturing, we have started from gigantic machines that filled an entire room, to low-cost tiny microchips that billons of people can afford and keep in their pockets (or should I say, hands?) all day long. Still, even with this level of progress, mobile devices are barely capable of replicating the "brain" of a jellyfish, and the trend shows that we are already hitting our limits in semiconductor scaling. In this paper, we define the Cost-Performance Ratio (CPR) metric that captures the trend in a single equation. We propose that we shall find solutions in each area of intra-chip, inter-chip, and inter-device level, and highlight the domain-specific computing, 3D packaging, and advanced communication as the main drivers to the next level of computing, satisfying our insatiable need.

11:50 AM

Presentations to Plenary Speakers

11:55 AM

Conclusion

Processors

Session Chair: Hugh Mair, *Mediatek, Fairview, TX*
Session Co-Chair: Shidhartha Das, *ARM, Cambridge, United Kingdom*

1:30 PM

2.1 Ponte Vecchio: A Multi-Tile 3D Stacked Processor for Exascale Computing

W. Gomes[1], A. Koker[2], P. Stover[3], D. Ingerly[1], S. Siers[2], S. Venkataraman[4], C. Pelto[1], T. Shah[5], A. Rao[2], F. O'Mahony[1], E. Karl[1], L. Cheney[2], I. Rajwani[2], H. Jain[4], R. Cortez[2], A. Chandrasekhar[4], B. Kanthi[4], R. Koduri[6], [1]Intel, Portland, OR; [2]Intel, Folsom, CA; [3]Intel, Chandler, AZ; [4]Intel, Bengalur, India [5]Intel, Austin, TX; [6]Intel, Santa Clara, CA

2:00 PM

2.2 Sapphire Rapids: The Next-Generation Intel Xeon Scalable Processor

N. Nassif[1], A. O. Munch[1], C. L. Molnar[1], G. Pasdast[2], S. V. Iyer[2], Z. Yang[1], O. Mendoza[1], M. Huddart[1], S. Venkataraman[3], R. Marom[4], A. M. Kern[1], B. Bowhill[1], D. R. Mulvihill[5], S. Nimmagadda[3], V. Kalidindi[1], J. Krause[1], M. M. Haq[1], R. Sharma[1], K. Duda[5], [1]Intel, Hudson, MA; [2]Intel, Santa Clara, CA [3]Intel, Bangalore, India; [4]Intel, Haifa, Israel; [5]Intel, Fort Collins, CO

2:30 PM

2.3 IBM Telum: A 16-Core 5+ GHz DCM

O. Geva[1], C. Berry[1], R. Sonnelitter[1], D. Wolpert[1], A. Collura[1], T. Strach[2], D. Phan[1], C. Lichtenau[2], A. Buyuktosunoglu[3], H. Harrer[2], J. Zitz[1], C. Marquart[1], D. Malone[1], T. Webel[2], A. Jatkowski[1], J. Isakson[4], D. Hamid[1], M. Cichanowski[4], M. Romain[1], F. Hasan[4], K. Williams[1], J. Surprise[1], C. Cavitt[1], M. Cohen[1]
[1]IBM Systems and Technology, Poughkeepsie, NY
[2]IBM Systems and Technology, Boeblingen, Germany
[3]IBM Research, Yorktown Heights, NY; [4]IBM Systems and Technology, Austin, TX

Break 3:00 PM

3:15 PM

2.4 POWER10™: A 16-Core SMT8 Server Processor with 2TB/s Off-Chip Bandwidth in 7nm Technology

R. M. Rao[1], C. Gonzalez[2], E. Fluhr[3], A. Mathews[3], A. Bianchi[3], D. Dreps[3], D. Wolpert[4], E. Lai[3], G. Strevig[3], G. Wiedemeier[3], P. Salz[5], R. Kruse[3], [1]IBM, Bengaluru, India; [2]IBM, Yorktown Heights, NY [3]IBM, Austin, TX; [4]IBM, Poughkeepsie, NY; [5]IBM, Boblingen, Germany

3:45 PM

2.5 A 5nm 3.4GHz Tri-Gear ARMv9 CPU Subsystem in a Fully Integrated 5G Flagship Mobile SoC

A. Nayak[1], H. Chen[1], H. Mair[1], R. Lagerquist[1], T. Chen[1], A. Rajagopalan[1], G. Gammie[1], R. Madhavaram[1], M. Jagota[1], C. Chung[1], J. Wiedemeier[1], B. Meera[1], C-Y. Yeh[2], M. Lin[2], C. Lin[2], V. Lin[2], J. Lin[2], Y. Chen[2], B. Chen[2], C-Y. Wu[2], R. ChangChien[2], R. Tzeng[2], K. Yang[2], A. Thippana[1], E. Wang[2], S. Hwang[2]
[1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan

4:15 PM

2.6 A 16nm 785GMACs/J 784-Core Digital Signal Processor Array with a Multilayer Switch Box Interconnect, Assembled as a 2×2 Dielet with 10µm-Pitch Inter-Dielet I/O for Runtime Multi-Program Reconfiguration

U. Rathore, S. S. Nagi*, S. Iyer, D. Marković*, *Equally-Credited Authors (ECAs)
University of California, Los Angeles, CA

4:45 PM

2.7 Zen3: The AMD 2nd-Generation 7nm x86-64 Microprocessor Core

T. Burd[1], W. Li[1], J. Pistole[1], S. Venkataraman[1], M. McCabe[1], T. Johnson[1], J. Vinh[1], T. Yiu[1], M. Wasio[1], H-H. Wong[1], D. Lieu[1], J. White[2], B. Munger[2], J. Lindner[2], J. Olson[2], S. Bakke[2], J. Sniderman[2], C. Henrion[3], R. Schreiber[4], E. Busta[3], B. Johnson[3], T. Jackson[3], A. Miller[3], R. Miller[3], M. Pickett[3], A. Horiuchi[3], J. Dvorak[3], S. Balagangadharan[5], S. Ammikkallingal[5], P. Kumar[5]
[1]AMD, Santa Clara, CA; [2]AMD, Boxborough, MA; [3]AMD, Fort Collins, CO; [4]AMD, Austin, TX
[5]AMD, Bangalore, India

Conclusion 5:15 PM

Analog Techniques & Sensor Interfaces

Session Chair: Viola Schaffer, *Texas Instruments, Freising, Germany*
Session Co-Chair: Jiawei Xu, *Fudan University, Shanghai, China*

1:30 PM

3.1 A Single-Crystal-Oscillator-Based Clock-Management IC with 18× Start-Up Time Reduction and 0.68ppm/°C Duty-Cycled Machine-Learning-Based RCO Calibration

J. Jung, S. Oh, J. Kim, G. Ha, J. Lee, S. Kim, E. Park, J. Lee, Y. Yoon, S. Bae, W. Kim, Y. Lim, K. Lee, J. Huh, J. Lee, T. B. Cho
Samsung Electronics, Hwaseong, Korea

2:00 PM

3.2 A 52MHz -158.2dBc/Hz PN @ 100kHz Digitally Controlled Crystal Oscillator Utilizing a Capacitive-Load-Dependent Dynamic Feedback Resistor in 28nm CMOS

J. Jung, S. Kim, W. Kim, J. Han, E. Park, S. Hwang, S. Oh, S. Han, K. Lee, J. Huh, J. Lee
Samsung Electronics, Hwaseong, Korea

2:30 PM

3.3 A 174μV Input Noise, 1GS/s Comparator in 22nm FDSOI with a Dynamic-Bias Preamplifier Using Tail Charge Pump and Capacitive Neutralization Across the Latch

H. S. Bindra, J. Ponte, B. Nauta
University of Twente, Enschede, The Netherlands

2:45 PM

3.4 A Second-Order Temperature-Compensated On-Chip R-RC Oscillator Achieving 7.93ppm/°C and 3.3pJ/Hz in -40°C to 125°C Temperature Range

Y. Ji[1,2], J. Liao[1], S. Arjmandpour[1,3], A. Novello[1], J-Y. Sim[2], T. Jang[1]
[1]ETH Zürich, Zürich, Switzerland
[2]Pohang University of Science and Technology, Pohang, Korea
[3]Sharif University of Technology, Tehran, Iran

Break 3:00 PM

3:15 PM

3.5 A ±25A Versatile Shunt-Based Current Sensor with 10kHz Bandwidth and ±0.25% Gain Error from –40°C to 85°C Using 2-Current Calibration

Z. Tang[1], R. Zamparette[1], Y. Furuta[2], T. Nezuka[2], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]MIRISE Technologies, Aichi, Japan

3:45 PM

3.6 A MEMS Coriolis-Based Mass-Flow-to-Digital Converter with 100μg/h/√Hz Noise Floor and Zero Stability of ±0.35mg/h

A. C. de Oliveira, S. Pan, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

4:15 PM

3.7 A 2.6mW 10pT/√Hz 33kHz Magnetoimpedance-Based Magnetometer with Automatic Loop-Gain and Bandwidth Enhancement

I. Akita[1], T. Kawano[2], H. Aoyama[2], S. Tatematsu[2], M. Hioki[1]
[1]Advanced Industrial Science and Technology (AIST), Tsukuba, Japan
[2]Aichi Steel, Tohkai, Japan

4:45 PM

3.8 A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of ±0.45°C (3σ) from -50°C to 180°C and a Resolution-FoM of 7.2pJ·K² at 150°C

B. Wang[1], M-K. Law[2], A. Bermak[1]
[1]Hamad Bin Khalifa University, Doha, Qatar
[2]University of Macau, Macau, China

Conclusion 5:15 PM

mm-Wave and SubTHz ICs for Communication and Sensing

Session Chair: Yiwu Tang, *Qualcomm Technologies, San Diego, CA*
Session Co-Chair: Ho-Jin Song, *POSTECH, Pohang, Korea*

1:30 PM

4.1 Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules

M. Elkhouly[1], J. Ha[1], M. J. Holyoak[1], D. Hendry[2], M. Sayginer[1], R. Enright[1], I. Kimionis[1], Y. Baeyens[1], S. Shahramian[1]

[1]Nokia Bell Labs, New Providence, NJ; [2]L3 Harris, QLD, Australia

2:00 PM

4.2 A Fully Integrated 160Gb/s D-Band Transmitter with 1.1pJ/b Efficiency in 22nm FinFET Technology

S. Callender[1], A. Whitcombe*[1], A. Agrawal*[1], R. Bhat[1], M. Rahman[2], C. C. Lee[3], P. Sagazio[1], G. Dogiamis[4], B. Carlton[1], M. Chakravorti[1], S. Pellerano[1], C. Hull[1],* *Equally-Credited Authors (ECAs)

[1]Intel, Hillsboro, OR; [2]now with IIT Delhi, New Delhi, India

[3]now with Nebula Microsystems, Richardson, TX; [4]Intel, Chandler, AZ

2:30 PM

4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and Adaptive Self-Interference Cancellation for FMCW Monostatic Radar

X. Chen[1], M. I. W. Khan[1], X. Yi[1,2], X. Li[1,3], W. Chen[3], J. Zhu[4], Y. Yang[4], K. E. Kolodziej[5], N. M. Monroe[1], R. Han[1]

[1]Massachusetts Institute of Technology, Cambridge, MA

[2]South China University of Technology, Guangzhou, China; [3]Tsinghua University, Beijing, China

[4]University of Technology Sydney, Ultimo, Australia; [5]MIT Lincoln Laboratory, Lexington, MA

Break 3:00 PM

3:15 PM

4.4 A 23-to-29GHz Receiver with mm-Wave N-Input-N-Output Spatial Notch Filtering and Autonomous Notch-Steering Achieving 20-to-40dB mm-Wave Spatial Rejection and -14dBm In-Notch IP1dB

L. Zhang, M. Babaie, Delft University of Technology, Delft, The Netherlands

3:45 PM

4.5 Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction

N. M. Monroe[1], G. C. Dogiamis[2], R. Stingel[2], P. Myers[2], X. Chen[1], R. Han[1]

[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Intel Corporation, Chandler, AZ

4:15 PM

4.6 430GHz CMOS Concurrent Transceiver Pixel Array for High Angular Resolution Reflection-Mode Active Imaging

Y. Zhu[1], P. R. Byreddy[1], S. Dong[1], K. K. O[1], W. Choi[2]

[1]University of Texas, Dallas, TX; [2]Oklahoma State University, Stillwater, OK

4:45 PM

4.7 A 300GHz 52mW CMOS Receiver with On-Chip LO Generation

O. Memioglu, Y. Zhao, B. Razavi, University of California, Los Angeles, CA

5:00 PM

4.8 A 3.4mW/element Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation

X. Fu, Y. Wang, D. You, X. Wang, A. A. Fadila, Y. Zhang, S. Kato, C. Wang, Z. Li, J. Pang, A. Shirane, K. Okada

Tokyo Institute of Technology, Tokyo, Japan

Conclusion 5:15 PM

Imagers, Range Sensors and Displays

Session Chair: *Mutsumi Hamaguchi, Sharp, Tenri, Japan*

Session Co-Chair: Seong-Jin Kim, *Ulsan National Institute of Science and Technology, Ulsan, Korea*

1:30 PM

5.1 A 0.37W 143dB-Dynamic-Range 1Mpixel Backside-Illuminated Charge-Focusing SPAD Image Sensor with Pixel-Wise Exposure Control and Adaptive Clocked Recharging

Y. Ota, K. Morimoto, T. Sasago, M. Shinohara, Y. Kuroda, W. Endo, Y. Maehashi, S. Maekawa, H. Tsuchiya, A. Abdelghafar, S. Hikosaka, M. Motoyama, K. Tojima, K. Uehira, J. Iwata, F. Inui, Y. Matsuno, K. Sakurai, T. Ichikawa, Canon, Kanagawa, Japan

2:00 PM

5.2 A 64×64-Pixel Flash LiDAR SPAD Imager with Distributed Pixel-to-Pixel Correlation for Background Rejection, Tunable Automatic Pixel Sensitivity and First-Last Event Detection Strategies for Space Applications

E. Manuzzato[1], A. Tontini[1], A. Seljak[1,2], M. Perenzoni[1]

[1]Fondazione Bruno Kessler, Trento, Italy; [2]Jozef Stefan Institute, Ljubljana, Slovenia

2:30 PM

5.3 An 80×60 Flash LiDAR Sensor with In-Pixel Histogramming TDC Based on Quaternary Search and Time-Gated Δ-Intensity Phase Detection for 45m Detectable Range and Background Light Cancellation

S. Park[1], B. Kim[1], J. Cho[2], J-H. Chun[2,3], J. Choi[2,3], S-J. Kim[1]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea; [2]SolidVue, Suwon, Korea

[3]Sungkyunkwan University, Suwon, Korea

Break 3:00 PM

3:15 PM

5.4 A 38μm Range Precision Time-of-Flight CMOS Range Line Imager with Gating Driver Jitter Reduction Using Charge-Injection Pseudo Photocurrent Reference

K. Yasutomi, T. Furuhashi, K. Sagawa, T. Takasawa, K. Kagawa, S. Kawahito

Shizuoka University, Hamamatsu, Japan

3:45 PM

5.5 A 1/1.57-inch 50Mpixel CMOS Image Sensor with 1.0μm All-Directional Dual Pixel by 0.5μm-Pitch Full-Depth Deep-Trench Isolation Technology

T. Jung, M. Fujita, J. Cho, K. Lee, D. Seol, S. An, C. Lee, Y. Jeong, M. Jung, S. Park, S. Baek, S. Jung, S. Lee, J. Yun, E. S. Shim, H. Han, E. Park, H. Sul, S. Kang, K. Lee, J. Ahn, D. Chang

Samsung Electronics, Hwasung, Korea

4:00 PM

5.6 A 4.9Mpixel Programmable-Resolution Multi-Purpose CMOS Image Sensor for Computer Vision

H. Murakami[1], E. Bohannon[1], J. Childs[1], G. Gui[1], E. Moule[1], K. Hanzawa[2], T. Koda[1], C. Takano[2], T. Shimizu[3], Y. Takizawa[3], A. Basavalingappa[1], R. Childs[1], C. Cziesler[1], R. Jarnot[1], K. Nishimura[3], S. Rogerson[1], Y. Nitta[1],

[1]Sony Electronics, San Jose, CA; [2]Sony Semiconductor Solutions, Atsugi, Japan

[3]Sony LSI Design, Atsugi, Japan

4:15 PM

5.7 A Fully Digital Time-Mode CMOS Image Sensor with 22.9pJ/frame·pixel and 92dB Dynamic Range

S. Kim, T. Kim, K. Seo, G. Han, Yonsei University, Seoul, Korea

4:45 PM

5.8 A 64Mpixel CMOS Image Sensor with 0.56μm Unit Pixels Separated by Front Deep-Trench Isolation

S. Park, C. Lee, S. Park, H. Park, T. Lee, D. Park, M. Heo, I. Park, H. Yeo, Y. Lee, J. Lee, B. Lee, D-C. Lee, J. Kim, B. Kim, J. Pyo, S. Quan, S. You, I. Ro, S. Choi, S-I. Kim, I-S. Joe, J. Park, C-H. Koo, J-H. Kim, C. K. Chang, T. Kim, J. Kim, J. Lee, H. Kim, C-R. Moon, H-S. Kim, Samsung Electronics, Hwaseong, Korea

5:00 PM

5.9 A 10b Source-Driver IC with LSB-Stacked LV-to-HV-Amplify DAC Achieving 2688μm²/channel and 4.8mV DVO for Mobile OLED Displays

G-W. Lim[1], G-G. Kang[1], H. Ma[2], M. Jeong[2], H-S. Kim[1]

[1]KAIST, Daejeon, Korea; [2]Samsung Display, Yongin, Korea

Conclusion 5:15 PM

Ultra-High-Speed Wireline

Session Chair: Thomas Toifl, *Cisco Systems, Thalwil, Switzerland*
Session Co-Chair: Amir Amirkhany, *Samsung Display America Lab, San Jose, CA*

1:30 PM

6.1 A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation

Y. Segal[1], A. Laufer[1], A. Khairi[1], Y. Krupnik[1], M. Cusmai[1], I. Levin[1], A. Gordon[1], Y. Sabag[1], V. Rahinski[1], G. Ori[1], N. Familia[1], S. Litski[1], T. Warshavsky[1], U. Virobnik[1], Y. Horwitz[1], A. Balankutty[2], S. Kiran[2], S. Palermo[3], P. M. Li[4], A. Cohen[1]
[1]Intel, Jerusalem, Israel; [2]Intel, Hillsboro, OR; [3]Texas A&M University, College Station, TX
[4]Intel, San Jose, CA

2:00 PM

6.2 A 112.5Gb/s ADC-DSP-Based PAM-4 Long-Reach Transceiver with >50dB Channel Loss in 5nm FinFET

Z. Guo[1], A. Mostafa[1], A. Elshazly[1], B. Chen[1], B. Wang[1], C. Han[1], C. Wang[1], D. Zhou[1], D. Visani[1], E. Hsiao[1], F. Chu[1], F. Lu[1], G. Cui[1], H. Zhang[1], H. Wang[1], H. Zhao[1], J. Lin[1], J. Gu[1], L. Luo[2], L. Jiang[1], M. Singh[1], M. Gambhir[1], M. Hasan[1], M. Wu[1], M. J. Yoo[1], P. Liu[1], S. Kollu[1], T. Ye[2], X. Zhao [2], X. Yang[1], Y. Huang[1], X. Han[1], Y. Sun[1], Z. Yu[1], Z. H. Jiang [1], Z. Adal[1], Z. Yan[1]
[1]Marvell, Santa Clara, CA; [2]Marvell, Shanghai, China

2:30 PM

6.3 A 2.29pJ/b 112Gb/s Wireline Transceiver with RX 4-Tap FFE for Medium-Reach Applications in 28nm CMOS

B. Ye, K. Sheng, W. Gai, H. Niu, B. Zhang, Y. He, S. Jia, C. Chen, J. Yu
Peking University, Beijing, China

Break 3:00 PM

3:15 PM

6.4 An 182mW 1-60Gb/s Configurable PAM-4/NRZ Transceiver for Large Scale ASIC Integration in 7nm FinFET Technology

N. Kocaman[1], U. Singh[1], B. Raghavan[1], A. Iyer[1], K. Thasari[1], S. Surana[1], J. W. Jung[1], J. Jeong[1], H. Zhang[1], A. Vasani[1], Y. Shim[1], Z. Huang[1], A. Garg[1], H-B. Lee[1], B. Wu[2], F. Liu[1], R. Wang[1], M. Loh[2], A. Wang[2], M. Caresosa[1], B. Zhang[1], A. Momtaz[1]
[1]Broadcom, Irvine, CA; [2]Broadcom, San Jose, CA

3:45 PM

6.5 A 1.6Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Dynamic Receiver-Driven Adaptation of TX-FFE and Programmable Roaming Taps in 5nm CMOS

G. Gangasani[1], D. Hanson[1], D. Storaska[1], H. H. Xu[1], M. Kelly[1], M. Shannon[1], M. Sorna[1], M. Wielgos[1], P. B. Ramakrishna[2], S. Shi[3], S. Parker[1], U. K. Shukla[2], W. Kelly[1], W. Su[3], Z. Yu[4]
[1]Marvell, Hopewell Junction, NY; [2]Marvell, Bangalore, India; [3]Marvell, Shanghai, China
[4]Marvell, Santa Clara, CA

4:15 PM

6.6 A 1-58.125Gb/s, 5-33dB IL Multi-Protocol Ethernet-Compliant Analog PAM-4 Receiver with 16 DFE Taps in 10nm

B. Zand, M. Bichan, A. Mahmoodi, M. Shashaani, J. Wang, R. Shulyzki, J. Guthrie, K. Tyshchenko, J. Zhao, E. Liu, N. Soltani, R. Anand, S. Rubab, R. Khela, S. Sharifian, K. Herterich
Intel, Toronto, Canada

4:45 PM

6.7 A 50Gb/s PAM-4 Bi-Directional Plastic Waveguide Link with Carrier Synchronization Using PI-Based Costas Loop

H-I. Song[1], H. Choi[1,2], J. Y. Yoo[1], H-S. Won[1], C. M. Lee[1], H. Jin[1], T. Y. Kim[1], W. Kwon[2], K. Lim[1], K. Kwon[1], C-A. Kim[1], T. Kim[1], J. G. Jo[1], J. Eu[1], S. Park[1], H-M. Bae[2]
[1]Point2 technology, Seoul, Korea; [2]KAIST, Daejeon, Korea

Conclusion 5:15 PM

NAND Flash Memory

Session Chair: Violante Moschiano, *Micron Semiconductor, Avezzano, Italy*
Session Co-Chair: Seung-Jae Lee, *Samsung, Hwasung-si, Kyeonggi-do, Korea*

3:15 PM

7.1 A 1-Tb 4b/Cell 4-Plane 3D Flash with 162-Layer 68-mm² Chip Size and 2.4-Gbps IO Speed

J. H. Yuh[1], J. Li[1], H. Li[1], Y. Oyama[1], C. Hsu[1], P. Anantula[2], S. Jeong[1], A. Amarnath[1], S. Darne[1], S. Bhatia[2], T. Tang[1], A. Arya[2], N. Rastogi[2], N. Ookuma[3], H. Mizukoshi[3], A. Yap[1], D. Wang[1], S. Kim[1], Y. Wu[1], M. Peng[1], J. Lu[1], T. Ip[1], S. Malhotra[2], D. Han[1], M. Okumura[1], J. Liu[1], J. Sohn[1], H. Chibvongodze[3], M. Balaga[2], A. Matsuda[1], C. Puri[2], C. Chen[1], I. K V[2], C. G[2], V. Ramachandra[1], Y. Kato[3], H. Wang[1], F. Moogat[1], I-S. Yoon[1], K. Kanda[4], T. Shimizu[4], N. Shibata[4], T. Shigeoka[4], K. Yanagidaira[4], T. Kodama[4], R. Fukuda[4], Y. Hirashima[4], M. Abe[4]
[1]Western Digital, Milpitas, CA
[2]Western Digital, Bangalore, India
[3]Western Digital, Yokohama, Japan
[4]KIOXIA, Tokyo, Japan

3:45 PM

7.2 A 1 Tb density 4b/Cell 3D NAND Flash on 176 Tier Technology with 4 Independent Planes for Read using CMOS Under the Array

T. Pekny[1], L. Vu[1], J. Tsai[1], D. Srinivasan[1], E. Yu[1], J. Pabustan[1], J. Xu[1], S. Deshmukh[1], K-F. Chan[1], M. Piccardi[1], K. Xu[1], G. Wang[1], K. Shakeri[1], V. Patel[1], T. Iwasaki[1], T. Wang[1], P. Musunuri[1], C. Gu[1], A. Mohammadzadeh[1], A. Ghalam[1], V. Moschiano[2], T. Vali[2], J. Park[1], J. Lee[1], R. Ghodsi[1]
[1]Micron Technology, San Jose, CA
[2]Micron Technology, Avezzano, Italy

4:15 PM

7.3 A 1Tb 4b/Cell, 176 Stacked WL 3D NAND Flash Memory with Improved Read Latency and 14.8Gb/mm² Area Density

W. Cho, J. Jung, J. Kim, J. Ham, S. Lee, Y. Noh, D. Kim, W. Lee, K. Cho, K. Kim, H. Lee, S. Chai, E. Jo, H. Cho, J-S. Kim, C. Kwon, C. Park, H. Nam, H. Won, T. Kim, K. Park, S. Oh, J. Ban, J. Park, J. Shin, T. Shin, J. Jang, J. Mun, J. Choi, H. Choi, S-W. Choi, W. Park, D. Yoon, M. Kim, J. Lim, C. An, H. Shim, H. Oh, H. Park, S. Shim, H. Huh, H. Choi, S. Lee, J. Sim, K. Gwon, J. Kim, W. Jeong, J. Choi, K-W. Jin
SK hynix, Icheon, Korea

4:45 PM

7.4 A 1Tb 3-bit/Cell 8th-Generation 3D NAND Flash Memory with 164MB/s Write Throughput and 2.4Gb/s Interface

M. Kim, H. K. Park, J. Lee, Y. S. Kim, D. Na, S. Choi, S. W. Yun, Y. Song, J. Lee, H. Yoon, K. Lee, B. Jeong, J. Park, S. Kim, J. Park, C. A. Lee, J. Lee, J. Lee, J. Y. Chun, J. Jang, Y. Yang, S. H. Moon, M. Choi, W. Kim, J. Kim, S. Yoon, P. Kwak, M. Lee, R. Song, S. Kim, C. Yoon, D. C. Kang, J-Y. Lee, J. Song
Samsung Electronics, Hwaseong, Korea

5:00 PM

7.5 A 512Gb In-Memory-Computing 3D NAND Flash Supporting Similar Vector Matching Operations on AI Edge Devices

H-W. Hu[1,2], W-C. Wang[1,3], C-K. Chen[1], Y-C. Lee[1], B-R. Lin[1], H-M. Wang[1], Y-P. Lin[1], Y-C. Lin[1], C-C. Hsieh[1], C-M. Hu[1], Y-T. Lai[1], H-S. Chen[1], Y-H. Chang[4], H-P. Li[1], T-W. Kuo[3,5], K-C. Wang[1], M-F. Chang[2], C-H. Hung[1], C-Y. Lu[1]
[1]Macronix, Hsinchu, Taiwan
[2]National Tsing Hua University, Hsinchu, Taiwan
[3]National Taiwan University, Taipei, Taiwan
[4]Academia Sinica, Taipei, Taiwan
[5]City University of Hong Kong, Hong Kong, China

Conclusion 5:15 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 21st, and Tuesday February 22nd, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022.

List of Papers to Come.

EE3: Semiconductor Supply Chain

Organizers: **Rahul M. Rao**, *IBM, Bangalore, India*

Co-Organizers: **Mijunh Noh,** *Samsung Electronics, Hwaseong-si, Korea*
Massimo Alioto, *National University of Singapore, Singapore*
Chia-Hsiang Yang, *National Taiwan University, Taipei, Taiwan*

Moderator: **Jimmy Goodrich**, *Semiconductor Industry Association, Washington, DC*

The Semiconductor supply chain is a highly specialized global complex system stretching from design houses to manufacturing fabs, to test and assembly units, and integration factories, which varies by the nature of the company, market and product. The pandemic of 2020, with component shortages, along with the geopolitical trade conflicts, and the threat of counterfeiting, have highlighted the challenges and need for a better orchestrated and diversified management chain. This panel will highlight the risks ahead, and ways to get ahead of these challenges through market awareness, transparency, open platforms, global supplier landscape, and academic research.

Panelists:
Shawn Han, *Samsung Foundry, Seoul, Korea*
Jung Yoon, *IBM, Poughkeepsie, NY*
Bindiya Vakil, *Resilinc, Milpitas, CA*
Michael Reiha, *Soitec Microelectronics, Singapore*
Fredrik Tillman, *Ericsson, Lund, Sweden*
Willy C. Shih, *Harvard Business School, Boston, MA*

EE4: The Bright and Dark Side of Artificial Intelligence (AI)

Co-Organizers: **Denis Daly,** *Apple, Cambridge, MA*
Sriram Vangal, *Intel, Hillsboro, OR*
Jae-sun Seo, *Arizona State University, Tempe, AZ*

Moderator: **Tinoosh Mohsein**, *University of Maryland, Baltimore, MD*

What is the golden vision for futuristic AI platforms? What are compelling AI use-cases and where are the risks? For instance, AI holds a great deal of promise for cybersecurity and human-centric robots. However, these sectors also have some of the highest potential for fallout. The panel will discuss forward-looking policy developments and ethical, legal, and societal issues related to AI, including socio-economic challenges.

Panelists:
Kailash Gopalakrishnan, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Evgeni Gousev, *Qualcomm, San Diego, CA*
Nele Mentens, *KU Leuven, Leuven, Belgium, and Leiden University, Leiden, The Netherlands*
Robert Muchsel, *Analog Devices, Dallas, TX*
Lama Nachman, *Intel, Santa Clara, CA*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*

Advanced RF Building Blocks

Session Chair: Hua Wang, *ETH Zurich, Zurich, Switzerland, Switzerland*
Session Co-Chair: Masoud Babaie, *Delft University of Technology, Delft, The Netherlands*

8:30 AM

8.1 A 0.0078mm² 3.4mW Wideband Positive-Feedback-Based Noise-Cancelling LNA in 28nm CMOS Exploiting G_m Boosting

Z. Liu, C. C. Boon, C. Li, K. Yang, Y. Dong, T. Guo
Nanyang Technological University, Singapore, Singapore

9:00 AM

8.2 A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup

S. Kundu, T. Huusari, H. Luo, A. Agrawal, E. Alban, S. Shahraini, T. Xiong, D. Lake, S. Pellerano, J. Mix, N. Kurd, M. Abdel-moneum, B. Carlton
Intel, Hillsboro, OR

9:30 AM

8.3 A 9-to-12GHz Coupled-RTWO FMCW ADPLL with 97fs RMS Jitter, -120dBc/Hz PN at 1MHz Offset, and with Retrace Time of 12.5ns and 2µs Chirp Settling Time

H. Shanan[1], D. Dalton[2], V. Chillara [3], P. Dato[4]
[1]Analog Devices, Somerset, NJ
[2]Xilinx, Cork, Ireland
[3]Vishay, Cork, Ireland
[4]Bosch, Valencia, Spain

Break 10:00 AM

High-Quality GHz-to-THz Frequency Generation and Radiation

Session Chair: Conan Zhan, *MediaTek, Hsinchu, Taiwan*
Session Co-Chair: Swami Sankaran, *Texas Instruments, Dallas, TX*

10:15 AM

9.1 Series-Resonance BiCMOS VCO with Phase Noise of -138dBc/Hz at 1MHz Offset from 10GHz and -190dBc/Hz FoM

A. Franceschin, D. Riccardi, A. Mazzanti
University of Pavia, Pavia, Italy

10:45 AM

9.2 A 0.049mm^2 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FoM$_A$ in 22nm FinFET

J. Gong[1,2], B. Patra[3], L. Enthoven[1,2], J. V. Staveren[1,2], F. Sebastiano[1,2], M. Babaie[1,2]
[1]Delft University of Technology, Delft, The Netherlands
[2]QuTech, Delft, The Netherlands
[3]Intel, Hillsboro, OR

11:15 AM

9.3 A 53.6-to-60.2GHz Many-Core Fundamental Oscillator with Scalable Mesh Topology Achieving -136.0dBc/Hz Phase Noise at 10MHz Offset and 190.3dBc/Hz Peak FoM in 65nm CMOS

H. Jia, R. Ma, W. Deng, Z. Wang, B. Chi
Tsinghua University, Beijing, China

11:45 AM

9.4 A Highly Power Efficient 2×3 PIN Diode-Based Intercoupled THz Radiating Array at 425GHz with 18.1dBm EIRP in 90nm SiGe BiCMOS

S. Razavian[1], A. Babakhani[2]
[1]University of California, Los Angeles, CA
[2]University of California, Los Angeles

Conclusion 12:15 PM

Nyquist and Incremental ADCs

Session Chair: Jan Westra, *Broadcom, Bunnik, The Netherlands*
Session Co-Chair: Ping Gui, *Southern Methodist University, Dallas, TX*

8:30 AM

10.1 A 10GS/s 8b 25fJ/c-s 2850um² Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology
J. Liu, M. Hassanpourghadi, M. S-W. Chen
University of Southern California, Los Angeles, CA

9:00 AM

10.2 A 0.82mW 14b 130MS/s Pipelined-SAR ADC with a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend
J-C. Wang, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

9:30 AM

10.3 A 0.004mm² 200MS/s Pipelined SAR ADC with kT/C Noise Cancellation and Robust Ring-Amp
M. Zhan[1], L. Jie[1], X. Tang[2], N. Sun[1]
[1]Tsinghua University, Beijing, China
[2]Peking University, Beijing, China

Break 10:00 AM

10:15 AM

10.4 A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment
H. Zhao, F. F. Dai
Auburn University, Auburn, AL

10:45 AM

10.5 A 24b 2MS/s SAR ADC with 0.03ppm INL and 106.3dB DR in 180nm CMOS
J. Steensgaard[1], R. Reay[2], R. Perry[2], D. Thomas[2], G. Tu[2], G. Reitsma[2]
[1]Analog Devices, Sequim, WA
[2]Analog Devices, Santa Clara, CA

11:15 AM

10.6 A 4.96µW 15b Self-Timed Dynamic-Amplifier-Based Incremental Zoom ADC
Y. Liu[1], M. Zhao[1], Y. Zhao[1], X. Yu[1], N. N. Tan[1], L. Ye[2], Z. Tan[1]
[1]Zhejiang University, Hangzhou, China
[2]Peking University, Beijing, China

11:45 AM

10.7 A 0.014mm² 10kHz-BW Zoom-Incremental-Counting ADC Achieving 103dB SNDR and 100dB Full-Scale CMRR
L. Jie[1], M. Zhan[1], X. Tang[2], N. Sun[1]
[1]Tsinghua University, Beijing, China
[2]Peking University, Beijing, China

Conclusion 12:15 PM

Compute-in-Memory and SRAM

Session Chair: Eric Karl, *Intel, Portland, OR*
Session Co-Chair: Yasuhiko Taito, *Renesas Electronics Corporation, Kodaira, Japan*

8:30 AM

11.1 A 1ynm 1.25V 8Gb, 16Gb/s/pin GDDR6-Based Accelerator-In-Memory Supporting 1TFLOPS MAC Operation and Various Activation Functions for Deep Learning Applications
S. Lee, K. Kim, S. Oh, J. Park, G. Hong, D. Ka, K. Hwang, J. Park, K. Kang, J. Kim, J. Jeon, N. Kim, Y. Kwon, K. Vladimir, W. Shin, J. Won, M. Lee, H. Joo, H. Choi, J. Lee, D. Ko, Y. Jun, K. Cho, I. Kim, C. Jeong, D. Kwon, J. Jang, I. Park, J. Chun, J. Cho, SK hynix, Icheon, Korea

9:00 AM

11.2 A 22nm 4Mb STT-MRAM data-encrypted Near-Memory-Computation Macro with 192GB/s Read-and-Decryption Bandwidth and 25.1-55.1 TOPS/W at 8b MAC for AI-oriented Operations
Y-C. Chiu[1], W-S. Khwa[2], C-S. Yang[1], S-H. Teng[1], H-Y. Huang[1], F-C. Chang[1], Y. Wu[1], Y-A. Chien[1], F-L. Hsieh[1], C-Y. Li[1], G-Y. Lin[1], P-J. Chen[1], T-H. Pan[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], C-P. Lo[2], Y-D. Chih[2], T-Y. J. Chang[2], M-F. Chang[1,2], [1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

9:30 AM

11.3 A 40nm 2M-cell 8b-Precision Hybrid SLC-MLC PCM Computing-in-Memory Macro with 20.5-65.0 TOPS/W for Tiny AI Edge Devices
W-S. Khwa[*1]*, Y-C. Chiu*[*2]*, C-J. Jhang[2], S-P. Huang[2], C-Y. Lee[2], T-H. Wen[2], F-C. Chang[2], S-M. Yu[1], T-Y. Lee[1], M-F. Chang[1,2]*, *Equally-Credited Authors (ECAs)
[1]TSMC Corporate Research, Hsinchu, Taiwan; [2]National Tsing Hua University, Hsinchu, Taiwan

Break 10:00 AM

10:15 AM

11.4 An 8Mb DC-Current-Free Binary-to-8b Precision ReRAM Nonvolatile Computing-in-Memory Macro using Time-Space-Readout with 1286.4 TOPS/W - 21.6 TOPS/W for AI Edge Devices
J-M. Hung[1], Y-H. Huang[1], S-P. Huang[1], F-C. Chang[1], T-H. Wen[1], C-I. Su[2], W-S. Khwa[2], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], Y-D. Chih[2], T-Y. J. Chang[2], M-F. Chang[1,2]
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

10:45 AM

11.5 Single-Mode 6T CMOS SRAM Macros with Keeper-Loading-Free Peripherals and Row-Separate Dynamic Body Bias Achieving 2.53fW/bit Leakage for AIoT Sensing Platforms
Y. Zhang[1], C. Xue[1], X. Wang[1], T. Liu[1], J. Gao[1], P. Chen[1], J. Liu[2], L. Sun[2], L. Shen[1], J. Ru[1], L. Ye[1,3], R. Huang[1]
[1]Peking University, Beijing, China; [2]Nano Core Chip Electronic Technology, Hangzhou, China
[3]Advanced Institute of Information Technology of Peking University, Hangzhou, China

11:00 AM

11.6 A 5 nm 254 TOPS/W and 221 TOPS/mm² Fully Digital Computing-in-Memory Supporting Wide Range Dynamic-Voltage-Frequency Scaling and Simultaneous MAC and Write Operations
H. Fujiwara[1], H. Mori[1], W-C. Zhao[1], M-C. Chuang[1], R. Naous[2], C-K. Chuang[1], T. Hashizume[3], D. Sun[1], C-F. Lee[1], K. Akarvardar[2], S. Adham[4], T-L. Chou[1], M. E. Sinangil[2], Y. Wang[1], Y-D. Chih[1], Y-H. Chen[1], H-J. Liao[1], T-Y. J. Chang[1]
[1]TSMC, Hsinchu, Taiwan; [2]TSMC, San Jose, CA; [3]TSMC, Yokohama, Japan; [4]TSMC, Austin, TX

11:15 AM

11.7 A 1.041Mb/mm² 27.38TOPS/W Signed-INT8 Dynamic Logic Based ADC-Less SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI and Embedded Applications
B. Yan[1], J-L. Hsu[2], P-C. Yu[2], C-C. Lee[2], Y. Zhang[3], W. Yue[1], G. Mei[3], Y. Yang[1], Y. Yang[2], H. Li[4], Y. Chen[4], R. Huang[1],
[1]Peking University, Beijing, China; [2]NeoNexus, Singapore, Singapore
[3]Pimchip Technology, Beijing, China; [4]Duke University, Durham, NC

11:45 AM

11.8 A 28nm 1Mb Time-Domain 6T SRAM Computing-in-Memory Macro with 6.6ns Latency 1241 GOPS and 37.01 TOPS/W for 8b-MAC Operations for AI Edge Devices
P-C. Wu[*1]*, J-W. Su*[*2]*, Y-L. Chung[1], L-Y. Hong[1], J-S. Ren[1], F-C. Chang[1], Y. Wu[1], H-Y. Chen[1], C-H. Lin[1], H-M. Hsiao[2], S-H. Li[2], S-S. Sheu[2], S-C. Chang[2], W-C. Lo[2], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], C-I. Wu[2], M-F. Chang[1]*
*Equally-Credited Authors (ECAs)
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]Industrial Technology Research Institute, Hsinchu, Taiwan

Conclusion 12:15 PM

Monolithic System for Robot and Bio Applications

Session Chair: Milin Zhang, *Tsinghua University, Beijing, China*
Session Co-Chair: Daniel Morris, *Meta, Menlo Park, CA*

8:30 AM

12.1 A 210 × 340 × 50µm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation

L. Xu[1], M. Lassiter[2], X. Wu[1], Y. Kim[1], J. Lee[1], M. Yasuda[3], M. Kawaminami[4], M. Miskin[2], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI; [2]University of Pennsylvania, Philadelphia, PA
[3]United Semiconductor Japan, Kuwana, Japan; [4]United Semiconductor Japan, Yokohama, Japan

9:00 AM

12.2 A 200 x 256 Image Sensor Heterogeneously Integrating a 2D Nanomaterial-Based Photo-FET Array and CMOS Time-to-Digital Converters

H. Hinton[1], H. Jang[1], W. Wu[1], M-H. Lee[2], M. Seol[2], H-J. Shin[2], S. Park[2], D. Ham[1]
[1]Harvard University, Cambridge, MA; [2]Samsung Advanced Institute of Technology, Suwon, Korea

9:30 AM

12.3 A Self-powering Wireless Soil-pH and Electrical Conductance Monitoring IC with Hybrid Microbial Electrochemical and Photovoltaic Energy Harvesting

C-Y. Wu[1], C-W. Liu[1], J-S. Chen[1], C-S. Huang[1], T-H. Lu[1], L-C. Chen[1], I-C. Ou[1], S-K. Lee[2], Y-C. Chen[2], P-H. Chen[1], C-T. Liu[2], Y-C. Liao[2], Y-T. Liao[1]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]National Taiwan University, Taipei, Taiwan

Break 10:00 AM

10:15 AM

12.4 A 256-Channel Actively-Multiplexed µECoG Implant with Column-Parallel Incremental ΔΣ ADCs Employing Bulk-DACs in 22-nm FDSOI Technology

X. Huang[1,2], H. Londoño-Ramírez[1,2,3], M. Ballini[4], C. Van Hoof[1,2], J. Genoe[1,2], S. Haesler[1,2,3,5], G. Gielen[1,2], N. Van Helleputte[1], C. Mora Lopez[1]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium
[3]Neuroelectronics Research Flanders, Leuven, Belgium; [4]TDK InvenSense, Milan, Italy
[5]Vlaams Instituut voor Biotechnologie, Leuven, Belgium

10:45 AM

12.5 A CMOS Cellular Interface Array for Digital Physiology Featuring High-Density Multi-Modal Pixels and Reconfigurable Sampling Rate

A. Y. Wang[1], Y. Sheng*[1], W. Li[2], D. Jung[3], G. Junek[1], J. Park[4], D. Lee[1], M. Wang[2], S. Maharjan[2], S. Kumashi[1], J. Hao[2], Y. S. Zhang[2], K. Eggan[2], H. Wang[1,5]*
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[1]Georgia Institute of Technology, Atlanta, GA; [2]Harvard University, Cambridge, MA
[3]Qualcomm, San Diego, CA; [4]Intel, Hillsboro, OR; [5]ETH Zürich, Zurich, Switzerland

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12.6 A CMOS Molecular Electronics Chip for Single-Molecule Biosensing

D. A. Hall[1], N. Ananthapadmanabhan[2], C. Choi[2], L. Zhang[2], P. P. Pan[2], C. W. Fuller[2], P. P. Padayatti[2], C. Gardner[2], D. Gebhardt[2], Z. Majzik[2], P. Sinha[2], P. W. Mola[2], B. Merriman[2]
[1]University of California, San Diego, CA; [2]Roswell Biotechnology, San Diego, CA

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12.7 1024 3D-Stacked Monolithic NEMS Array with 375µm2 0.5mW 0.28ppm Frequency Deviation Pixel-level Readout for Zeptogram Gravimetric Sensing

G. Billiot, P. Mattei, B. Vysotskyi, A. Reynaud, L. Hutin, C. Plantier, E. Rolland, M. Gely, G. Usai, C. Tabone, G. Pillonnet, S. Robinet, S. Hentz
CEA-Léti, Grenoble, France

Conclusion 12:15 PM

Digital Techniques for Clocking, Variation Tolerance and Power Management

Session Chair: Tanay Karnik, *Intel, Hillsboro, OR*
Session Co-Chair: Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*

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13.1 Clock Generator with ISO26262 ASIL-D Grade Safety Mechanism for SoC Clocking Application

D. Lim, S. Shin, S. Lee, K. Kwon, J. An, W. Yu, C. Jeong, W. Kim, M. Choi, J. Shin
Samsung Electronics, Hwaseong, Korea

9:00 AM

13.2 A 97fs$_{rms}$-Jitter and 68-Multiplication Factor, 8.16GHz Ring-Oscillator Injection-Locked Clock Multiplier with Power-Gating Injection-Locking and Background Multi-Functional Digital Calibrator

S. Park[*1], S. Yoo*[*2], Y. Shin[1], J. Lee[1], J. Choi[1]*
*Equally-Credited Authors (ECAs)
[1]KAIST, Daejeon, Korea; [2]Qualcomm, San Diego, CA

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13.3 A 0.021mm^2 65nm CMOS 2.5GHz Digital Injection-Locked Clock Multiplier with Injection Pulse Shaping Achieving -79dBc Reference Spur and 0.496mW/GHz Power Efficiency

R. Xu[1], D. Ye[1], S. Li[1], C-J. R. Shi[2]
[1]Fudan University, Shanghai, China; [2]University of Washington, Seattle, WA

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13.4 Fully Automated Hardware-Driven Clock-Gating Architecture with Complete Clock Coverage for 5nm Exynos Mobile SoC

J-G. Lee, H. Jeon, Y. Choi, A. Kim, Samsung Semiconductor, Hwaseong, Korea

Break 10:00 AM

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13.5 Deterministic Frequency Boost and Voltage Enhancements on the POWER10™ Processor

B. T. Vanderpool[1], P. J. Restle[2], E. J. Fluhr[3], G. S. Still[4], F. Campisano[3], I. Carmichael[3], E. Marz[5], R. Batra[3], R. Willaman[3]
[1]IBM, Rochester, MN; [2]IBM, Yorktown Heights, NY; [3]IBM, Austin, TX
[4]IBM, Research Triangle Park, NC; [5]IBM, Essex Junction, VT

10:45 AM

13.6 A 0.65V 1316µm^2 Fully Synthesizable Digital Temperature Sensor Using Wire Metal Achieving 0.16nJ·%^{2}-Accuracy FoM in 5nm FinFET CMOS

J. Park, J. Kim, K. Kim, J-H. Yang, M. Choi, J. Shin, Samsung Electronics, Gyeonggi, Korea

11:15 AM

13.7 Energy Minimization of Duty-Cycled Systems Through Optimal Stored-Energy Recycling from Idle Domains

C-H. Huang[1], A. Mandal[1], D. Peña-Colaiocco[1], E. Pereira Da Silva[2], V. Sathe[1]
[1]University of Washington, Seattle, WA; [2]NXP Semiconductors, Austin, TX

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13.8 A 194nW Energy-Performance-Aware IoT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization

X. Liu, S. Kamineni, J. Breiholz, B. H. Calhoun, S. Li, University of Virginia, Charlottesville, VA

Conclusion 12:15 PM

GaN, High-Voltage and Wireless Power

Session Chair: Bernhard Wicht, *University of Hannover, Hannover, Germany*
Session Co-Chair: Patrik Arno, *ST Microelectronics, Grenoble, France, Metropolitan*

8:30 AM

14.1 A Monolithic GaN-Based Driver and GaN Power HEMT with Diode-Emulated GaN Technique for 50MHz Operation and Sub-0.2ns Deadtime Control

Y-Y. Kao[1], T-W. Wang[1], S-H. Hung[1], Y-H. Wen[1], T-H. Yang[1], S-Y. Li[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

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14.2 A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control

C. Rindfleisch, B. Wicht, Leibniz University Hannover, Hannover, Germany

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14.3 A Monolithic GaN Direct 48V/1V AHB Switching Power IC with Auto-Lock Auto-Break Level Shifting, Self-Bootstrapped Hybrid Gate Driving, and On-Die Temperature Sensing

D. Yan, D. B. Ma, University of Texas, Dallas, TX

Break 10:00 AM

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14.4 A 2.5–5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor Assisted Dual Inductor Filtering

C. Chen, J. Liu, H. Lee, University of Texas, Dallas, TX

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14.5 2-Tx Digital Envelope-Tracking Supply Modulator Achieving 200MHz Channel Bandwidth and 93.6% Efficiency for 2G/3G/LTE/NR RF Power Amplifiers

J-S. Bang, D. Kim, J. Lee, S. Jung, Y. Choo, S. Park, Y-H. Jung, J-Y. Ko, T. Nomiyama, J. Baek, J. Han, S-H. Lee, I-H. Kim, J-S. Paek, J. Lee, T. B. Cho
Samsung Electronics, Hwaseong, Korea

11:15 AM

14.6 A 27W D2D Wireless Power Transfer System with Compact Single-Stage Regulated Class-E Architecture and Adaptive ZVS Control

X. Ma[1,2], Y. Lu[2], W-H. Ki[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]University of Macau, Macau, China

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14.7 A 1.2W 51%-Peak-Efficiency Isolated DC-DC Converter with a Cross-Coupled Shoot-Through-Free Class-D Oscillator Meeting the CISPR-32 Class-B EMI Standard

D. Pan[1], G. Li[1], F. Miao[1], W. Sun[1], X. Gong[2], L. Zhang[2], L. Cheng[1]
[1]University of Science and Technology of China, Hefei, China
[2]Suzhou Novosense Microelectronics, Suzhou, China

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14.8 A 68.3% Efficiency Reconfigurable 400-/800-mW Capacitive Isolated DC-DC Converter with Common-Mode Transient Immunity and Fast Dynamic Response by Through-Power-Link Hysteretic Control

J. Tang, L. Zhao, C. Huang, Iowa State university, Ames, IA

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ML Processors

Session Chair: SukHwan Lim, *Samsung Electronics, Hwaseong-si, Korea*
Session Co-Chair: Sophia Shao, *University of California, Berkeley, Berkeley, CA*

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15.1 A Multi-Mode 8K-MAC HW-Utilization-Aware Neural Processing Unit with a Unified Multi-Precision Datapath in 4nm Flagship Mobile SoC
J-S. Park[1], C. Park[1], S. Kwon[1], H-S. Kim[1], T. Jeon[1], Y. Kang[1], H. Lee[1], D. Lee[1], J. Kim[1], Y. Lee[1], S. Park[1], J-W. Jang[2], S. Ha[1], M. Kim[1], J. Bang[1], S. H. Lim[1], I. Kang[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]Samsung Advanced Institute of Technology, Suwon, Korea

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15.2 A 65nm Systolic Neural CPU Processor for Combined Deep Learning and General-Purpose Computing with 95% PE Utilization, High Data Locality and Enhanced End-to-End Performance
Y. Ju, J. Gu, Northwestern University, Evanston, IL

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15.3 COMB-MCM: Computing-on-Memory-Boundary NN Processor with Bipolar Bitwise Sparsity Optimization for Scalable Multi-Chiplet-Module Edge Machine Learning
H. Zhu[*1], B. Jiao*[*1], J. Zhang*[*1], X. Jia[1], Y. Wang[1], T. Guan[2], S. Wang[2], D. Niu[2], H. Zheng[2], C. Chen[1], M. Wang[1], L. Zhang[1], X. Zeng[1], Q. Liu[1], Y. Xie[2], M. Liu[1]*, *Equally-Credited Authors (ECAs)
[1]Fudan University, Shanghai, China; [2]Alibaba DAMO Academy, Shanghai, China

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15.4 Hiddenite: 4K-PE Hidden Network Inference 4D-Tensor Engine Exploiting On-Chip Model Construction Achieving 34.8-to-16.0TOPS/W for CIFAR-100 and ImageNet
K. Hirose, J. Yu*, K. Ando, Y. Okoshi, Á. López García-Arias, J. Suzuki, T. V. Chu, K. Kawamura, M. Motomura*, *Equally-Credited Authors (ECAs), Tokyo Institute of Technology, Yokohama, Japan

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15.5 A 28nm 29.2TFLOPS/W BF16 and 36.5TOPS/W INT8 Reconfigurable Digital CIM Processor with Unified FP/INT Pipeline and Bitwise In-Memory Booth Multiplication for Cloud Deep Learning Acceleration
F. Tu[1,2], Y. Wang[1], Z. Wu[1], L. Liang[2], Y. Ding[2], B. Kim[2], L. Liu[1], S. Wei[1], Y. Xie[2], S. Yin[1]
[1]Tsinghua University, Beijing, China; [2]University of California, Santa Barbara, CA

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15.6 DIANA: An End-to-End Energy-Efficient DIgital and ANAlog Hybrid Neural Network SoC
K. Ueyoshi[1], I. A. Papistas[2], P. Houshmand[1], G. M. Sarda[1,2], V. Jain[1], M. Shi[1], Q. Zheng[1], S. Giraldo[1], P. Vrancx[2], J. Doevenspeck[2], D. Bhattacharjee[2], S. Cosemans[2], A. Mallik[2], P. Debacker[2], D. Verkest[2], M. Verhelst[1,2], [1]KU Leuven, Leuven, Belgium; [2]imec, Leuven, Belgium

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15.7 ARCHON: A 332.7TOPS/W 5b Variation-Tolerant Analog CNN Processor Featuring Analog Neuronal Computation Unit and Analog Memory
J-O. Seo[1], M. Seok[2], S. Cho[1], [1]KAIST, Daejeon, Korea; [2]Columbia University, New York, NY

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15.8 Analog Matrix Processor for Edge AI Real-Time Video Analytics
L. Fick[1], S. Skrzyniarz[1], M. Parikh[1], M. B. Henry[2], D. Fick[1]
[1]Mythic, Austin, TX; [2]Mythic, Redwood City, CA

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15.9 A 0.8V Intelligent Vision Sensor with Tiny Convolutional Neural Network and Programmable Weights Using Mixed-Mode Processing-in-Sensor Technique for Image Classification
T-H. Hsu, G-C. Chen*, Y-R. Chen, C-C. Lo, R-S. Liu, M-F. Chang, K-T. Tang, C-C. Hsieh*
*Equally-Credited Authors (ECAs), National Tsing Hua University, Hsinchu, Taiwan

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Emerging Domain-Specific Digital Circuits and Systems

Session Chair: Huichu Liu, *Meta, Menlo Park, CA*
Session Co-Chair: Mijung Noh, *Samsung Electronics, Hwaseong-si, Korea*

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16.1 DIMC: 2219TOPS/W 2569F²/b Digital In-Memory Computing Macro in 28nm Based on Approximate Arithmetic Hardware

D. Wang[1], C-T. Lin[1], G. K. Chen[2], P. Knag[2], R. K. Krishnamurthy[2], M. Seok[1]
[1]Columbia University, New York, NY
[2]Intel, Portland, OR

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16.2 A 40nm 64kb 26.56TOPS/W 2.37Mb/mm² RRAM Binary/Compute-in-Memory Macro with 4.23× Improvement in Density and >75% Use of Sensing Dynamic Range

S. D. Spetalnick[1], M. Chang[1], B. Crafton[1], W-S. Khwa[2], Y-D. Chih[3], M-F. Chang[2], A. Raychowdhury[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Design Technology, Hsinchu, Taiwan

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16.3 A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems

M. Chang[1], S. D. Spetalnick[1], B. Crafton[1], W-S. Khwa[2], Y-D. Chih[3], M-F. Chang[2], A. Raychowdhury[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Design Technology, Hsinchu, Taiwan

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16.4 Flex6502: A Flexible 8b Microprocessor in 0.8µm Metal-Oxide Thin-Film Transistor Technology Implemented with a Complete Digital Design Flow Running Complex Assembly Code

H. Çeliker[1,2], A. Sou[3], B. Cobb[3], W. Dehaene[1,2], K. Myny[1,2]
[1]imec, Leuven, Belgium
[2]KU Leuven ESAT, Leuven, Belgium
[3]PragmatIC Semiconductor Ltd, Cambridge, United Kingdom

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16.5 FlexSpin: A Scalable CMOS Ising Machine with 256 Flexible Spin Processing Elements for Solving Complex Combinatorial Optimization Problems

Y. Su[1], T-H. Kim[1], B. Kim[2]
[1]Nanyang Technological University, Singapore, Singapore
[2]University of California, Santa Barbara, CA

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16.6 A 65nm 63.3µW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes

B. Chatterjee, A. Datta, M. Nath, G. K. K, N. Modak, S. Sen
Purdue University, West Lafayette, IN

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16.7 An Optimal Digital Beamformer for mm-Wave Phased Arrays with 660MHz Instantaneous Bandwidth in 28nm CMOS

D. Peña-Colaiocco, C-H. Huang, K-D. Chu, J. C. Rudell, V. Sathe
University of Washington, Seattle, WA

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Advanced Wireline Links and Techniques

Session Chair: Bo Zhang, *Broadcom, Irvine, CA*
Session Co-Chair: Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*

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17.1 A 4.6pJ/b 200Gb/s Analog DP-QPSK Coherent Optical Receiver in 28nm CMOS
K. Sheng, H. Niu*, B. Zhang*, W. Gai, B. Ye, H. Zhou, C. Chen*
*Equally-Credited Authors (ECAs)
Peking University, Beijing, China

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17.2 A 2.4pJ/b 100Gb/s 3D-Integrated PAM-4 Optical Transmitter with Segmented SiP MOSCAP Modulators and a 2-Channel 28nm CMOS Driver
A. Hashemi Talkhooncheh[1], W. Zhang[2], M. Wang[1], D. J. Thomson[2], M. Ebert[2], L. Ke[2], G. T. Reed[2], A. Emami[1]
[1]California Institute of Technology, Pasadena, CA
[2]University of Southampton, Southampton, United Kingdom

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17.3 A 10Gb/s Digital Isolator Using Coupled Split-Ring Resonators with 24kVpk Surge Capability and 100kV/μS Common-Mode Transient Immunity
J. Xu, R. Yun, B. Chen
Analog Devices, Wilmington, MA

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17.4 A 56GHz 23mW Fractional-N PLL with 110fs Jitter
Y. Zhao, O. Memioglu, B. Razavi
University of California, Los Angeles, CA

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17.5 A 480-Multiplication-Factor 13.2-to-17.3GHz Sub-Sampling PLL Achieving 6.6mW Power and -248.1dB FoM Using a Proportionally Divided Charge Pump
L. Zhang, A. Niknejad
University of California, Berkeley, CA

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17.6 A 65nm CMOS, 3.5-to-11GHz, Less-Than-1.45LSB-INL_{pp}, 7b Twin Phase Interpolator with a Wideband, Low-Noise Delta Quadrature Delay-Locked Loop for High-Speed Data Links
Z. Wang, P. R. Kinget
Columbia University, New York, NY

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17.7 A 9b-Linear 14GHz Integrating-Mode Phase Interpolator in 5nm FinFET Process
A. K. Mishra[1], Y. Li[2], P. Agarwal[2], S. Shekhar[1]
[1]University of British Columbia, Vancouver, Canada
[2]MaxLinear, Carlsbad, CA

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DC-DC Converters

Session Chair: Harish Krishnamurthy, *Intel, Hillsboro, OR*
Session Co-Chair: Xun Liu, *The Chinese University of Hong Kong, Shenzhen, Shenzhen, China*

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18.1 A 1.23W/mm² 83.7%-Efficiency 400MHz 6-Phase Fully-Integrated Buck Converter in 28nm CMOS with On-Chip Capacitor Dynamic Re-Allocation for Inter-Inductor Current Balancing and Fast DVS of 75mV/ns

J-H. Cho[1], D-K. Kim[1], H-H. Bae[1], Y-J. Lee[1,2], S-T. Koh[1], Y. Choo[2], J-S. Paek[2], H-S. Kim[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Hwaseong, Korea

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18.2 A 12V/24V-to-1V DSD Power Converter with 56mV Droop and 0.9µs 1% Settling Time for a 3A/20ns Load Transient

J. Yuan, Z. Liu, F. Wu, L. Cheng
University of Science and Technology of China, Hefei, China

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18.3 A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73x Theoretical Minimum Output Undershoot of DSD

T. Hu[1], M. Huang[1], Y. Lu[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

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18.4 A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning

P. H. McLaughlin, K. Datta, J. T. Stauth
Dartmouth College, Hanover, NH

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18.5 A 12 A Imax, Fully Integrated Multi-Phase Voltage Regulator with 91.5% Peak Efficiency at 1.8 to 1V, Operating at 50 MHz and Featuring a Digitally Assisted Controller with Automatic Phase Shedding and Soft Switching in 4nm Class FinFET CMOS

C. Schaef[1], T. Salus[2], R. Rayess[3], S. Kulasekaran[4], M. Manusharow[4], K. Radhakrishnan[4], J. Douglas[4]
[1]Intel, Hillsboro, OR; [2]Intel, Haifa, Israel; [3]Intel, Hudson, MA; [4]Intel, Chandler, AZ

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18.6 A 5V Input 98.4% Peak Efficiency Reconfigurable Capacitive-Sigma Converter with Greater than 90% Peak Efficiency for the Entire 0.4~1.2V Output Range

X. Yang, L. Zhao, M. Zhao, Z. Tan, L. He, Y. Ding, W. Li, W. Qu
Zhejiang University, Hangzhou, China

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18.7 A 2–5MHz Multiple DC Output Hybrid Boost Converter with Scalable CR Boosting Scheme Achieving 91% Efficiency at a Conversion Ratio of 12

C. Chen, J. Liu, H. Lee
University of Texas, Dallas, TX

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18.8 A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm² Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS

G. Cai[1], Y. Lu[1], R. Martins[1,2]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

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Power Amplifiers and Building Blocks

Session Chair: Hongtao Xu, *Fudan University, Shanghai, China*
Session Co-Chair: Yves Baeyens, *Nokia - Bell Labs, New Providence, NJ*

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19.1 A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier with Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-Off Efficiency

X. Li[1], W. Chen[1], S. Li[1], H. Wu[1], X. Yi[2], R. Han[3], Z. Feng[1]
[1]Tsinghua University, Beijing, China
[2]South China University of Technology, Guangzhou, China
[3]Massachusetts Institute of Technology, Boston, MA

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19.2 A 1V 32.1dBm 92-to-102GHz Power Amplifier with a Scalable 128-to-1 Power Combiner Achieving 15% Peak PAE in a 65nm Bulk CMOS Process

W. Zhu, J. Wang, R. Wang, J. Zhang, C. Li, S. Yin, Y. Wang
Tsinghua University, Beijing, China

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19.3 A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier with 20.4%/14.2% PAE at 6-/12-dB Power Back-Off and 25.5dBm P_{SAT} in 55nm Bulk CMOS

Z. Ma[1,2], K. Ma[1], K. Wang[1], F. Meng[1]
[1]Tianjin University, Tianjin, China
[2]University of Electronic Science and Technology of China, Chengdu, China

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19.4 A 26-to-39GHz Broadband Ultra-Compact High-Linearity Switchless Hybrid N/PMOS Bi-Directional PA/LNA Front-End for Multi-Band 5G Large-Scaled MIMO System

J. Park[1], H. Wang[1,2]
[1]Georgia Institute of Technology, Atlanta, GA
[2]ETH Zurich, Zurich, Switzerland

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19.5 A 16nm, +28dBm Dual-Band All-Digital Polar Transmitter Based on 4-core Digital PA for Wi-Fi6E Applications

B. Khamaisi[1], D. Ben-Haim[1], A. Nazimov[1], A. Ben-Bassat[1], S. Gross[1], N. Shay[1], G. Asa[1], V. Spector[1], Y. Eilat[1], A. Azam[2], E. Borokhovich[1], I. Shternberg[1], P. Skliar[1], E. Solomon[1], A. Beidas[1], T. A. Hazira[1], A. Lane[1], E. Shaviv[1], G. Nudelman[1], E. Dahan[1], M. Shemer[1], N. Kimiagarov[1], A. Ravi[2], O. Degani[1]
[1]Intel, Haifa, Israel
[2]Intel, Oregon, OR

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19.6 A Broadband Mm-Wave VSWR-Resilient Joint True Power Detector and Impedance Sensor Supporting Single-Ended Antenna Interfaces

D. J. Munzer[1], N. S. Mannem[1], E. Garay[1], H. Wang[1,2]
[1]Georgia Institute of Technology, Atlanta, GA
[2]ETH Zurich, Zurich, Switzerland

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19.7 A 1-to-18GHz Distributed-Stacked-Complementary Triple-Balanced Passive Mixer With up to 33dBm IIP3 and Integrated LO Driver in 45nm CMOS SOI

C. Hill[1,2], J. F. Buckwalter[2]
[1]LintrinsIC Semiconductors, Somerville, MA
[2]University of California, Santa Barbara, CA

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Body and Brain Interfaces

Session Chair: Sohmyung Ha, *New York University Abu Dhabi, Abu Dhabi, United Arab Emirates*
Session Co-Chair: Rikky Muller, *University of California, Berkeley, CA*

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20.1 A 0.5mΩ/√Hz 106dB SNR 0.45cm² Dry-Electrode Bioimpedance Interface with Current Mismatch Cancellation and Boosted Input Impedance of 100MΩ at 50kHz

Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, J. Xu, Fudan University, Shanghai, China

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20.2 A Time-Division Multiplexed 8-Channel Non-Contact ECG Recording IC with a Common-Mode Interference Tolerance of 20V_{PP}

K-J. Choi, J-Y. Sim, Pohang University of Science and Technology, Pohang, Korea

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20.3 A 0.7V 17fJ/step-FOM$_W$ 178.1dB-FOM$_{SNDR}$ 10kHz-BW 560mV_{PP} True-ExG Biopotential Acquisition System with Parasitic-Insensitive 421MΩ Input Impedance in 0.18µm CMOS

S. Lee[1], Y. Choi[1], G. Kim[1], S. Baik[1], T. Seol[1], H. Jang[1], D. Lee[1], M. Je[2], J-W. Choi[1], A. K. George[1], J. Lee[1]

[1]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea; [2]KAIST, Daejeon, Korea

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20.4 A 256-Channel 0.227µJ/class Versatile Brain Activity Classification and Closed-Loop Neuromodulation SoC with 0.004mm²-1.51µW/channel Fast-Settling Highly Multiplexed Mixed-Signal Front-End

U. Shin[1,2], L. Somappa[1], C. Ding[1], B. Zhu[1,2], Y. Vyza[1], A. Trouillet[1], S. P. Lacour[1,3], M. Shoaran[1,3]

[1]EPFL, Lausanne, Switzerland; [2]Cornell University, Ithaca, NY
[3]Center for Neuroprosthetics, Geneva, Switzerland

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20.5 A Miniaturized Wireless Neural Implant with Body-Coupled Data Transmission and Power Delivery for Freely Behaving Animals

C. Lee[,1], B. Kim*[,2], J. Kim[1], S. Lee[3,4], T. Jeon[1], W. Choi[1], S. Yang[3,4], J-H. Ahn[1], J. Bae[2], Y. Chae[1]*

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[2]Kangwon National University, Chuncheon, Korea; [3]Incheon National University, Incheon, Korea
[4]gBrain, Incheon, Korea

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20.6 A Reconfigurable Sub-Array Multiplexing Microelectrode Array System with 24,320 Electrodes and 380 Readout Channels for Investigating Neural Communication

J-H. Cha[1], J-H. Park[1], Y. Park[1], H. Shin[2], K. S. Hwang[2], I-J. Cho[2], S-J. Kim[1]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Korea Institute of Science and Technology, Seoul, Korea

4:30 PM

20.7 An SpO_2 Sensor Using Reconstruction-Free Sparse Sampling for 70% System Power Reduction

S. Faraji Alamouti[1], C. Yalcin[1], J. Jan[1], J. Ting[1], A. C. Arias[1], R. Muller[1,2]

[1]University of California, Berkeley, CA; [2]Chan Zuckerberg Biohub, San Francisco, CA

4:45 PM

20.8 A 145.2dB-DR Baseline-Tracking Impedance Plethysmogram IC for Neckband-Based Blood Pressure and Cardiovascular Monitoring

C. S. Park[1], H. Kim[1], K. Lee[1], D. S. Keum[2], D. P. Jang[3], J. J. Kim[1]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]SOSO H&C, Daegu, Korea; [3]Hanyang University, Seoul, Korea

Conclusion 5:15 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 21st, and Tuesday February 22nd, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2022.

List of Papers to Come.

ISSCC 2022 Timetable

Tutorials

T1: Analog Circuit Design in Bipolar-CMOS-DMOS (BCD) Technologies	**T2:** Fundamentals of High Frequency DC-DC Converters	**T3:** Noise-Shaping SAR ADCs
T4: Fundamentals of Self-Sensing Processing Systems	**T5:** Fundamentals of Process Monitors for Signoff-Oriented Circuit Design	**T6:** Wireless Power Transfer and Management for Medical Applications
T7: HBM DRAM and 3D Stacked Memory	**T8:** Fundamentals of Mixed-mode RF Transceivers	**T9:** Design Methodologies for Energy Harvesting Wireless Sensor Nodes
T10: Fundamentals of mm-Wave Phased-Arrays	**T11:** Basics of Equalization Techniques: Channels, Equalization, and Circuits	**T12:** Advances in Digital vs. Analog AI Accelerators

ISSCC 2022 • Sunday February 20th

Forums

8:00 AM	**F1:** Compute-in-X (CiX): Overcoming the Data Bottleneck in AI Processing	**F2:** Chip Design for Low-Power, Robust, and Secure IoT Devices

Events Below in Bold Box are Included with your Conference Registration

Special Events

	8:00 AM – SE1: Student Research Preview: Short Presentations with Poster Session	**7:50 AM – SE2:** Next Generation Circuit Designer 2022 Workshop

ISSCC 2022 • Monday February 21st • Paper Sessions

8:30 AM	**Session 1:** Plenary Session					
1:30 PM	**Session 2:** Processors	**Session 3:** Analog Techniques & Sensor Interfaces	**Session 4:** mmWave and SubTHz ICs for Communication and Sensing	**Session 5:** Imagers, Range Sensors and Displays	**Session 6:** Ultra-High-Speed Wireline	**3:15 PM Session 7:** NAND Flash Memory

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE3:** Semiconductor Supply Chain	**EE4:** The Bright and Dark Side of Artificial Intelligence (AI)

ISSCC 2022 • Tuesday February 22nd • Paper Sessions

8:30 AM	**Session 8:** Advanced RF Building Blocks **Session 9:** High-Quality GHz-to-THz Frequency Generation and Radiation	**Session 10:** Nyquist and Incremental ADCs	**Session 11:** Compute-in-Memory and SRAM	**Session 12:** Monolithic System for Robot and Bio Applications	**Session 13:** Digital Techniques for Clocking, Variation Tolerance and Power Management	**Session 14:** Gan, High-Voltage and Wireless Power
1:30 PM	**Session 15:** ML Processors	**Session 16:** Emerging Domain-Specific Digital Circuits and Systems	**Session 17:** Advanced Wireline Links and Techniques	**Session 18:** DC-DC Converters	**Session 19:** Power Amplifiers and Building Blocks	**Session 20:** Body and Brain Interfaces

10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE5:** Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?	**EE6:** Next Trillion Dollar Market

ISSCC 2022 • Wednesday February 23rd • Paper Sessions

8:30 AM	**10:15 AM Session 21:** Highlighted Chip Releases: Digital/ML	**Session 22:** Cryo-Circuits and Ultra-Low-Power Intelligent IoT	**Session 23:** Frequency Synthesizers	**Session 24:** Low-Power and UWB Radios for Communication and Ranging	**Session 25:** Noise-Shaping ADCs
1:30 PM	**Session 26:** Highlighted Chip Releases: Systems and Quantum Computing **Session 27:** mm-Wave & Sub-6GHz and Receivers and Transceivers for 5G Radios	**Session 28:** DRAM and Interface	**Session 29:** ML Chips for Emerging Applications **Session 30:** Power Management Techniques	**Session 31:** Audio Amplifiers **Session 32:** Ultrasound and Beamforming Applications	**Session 33:** Domain Specific Processors **Session 34:** Hardware Security

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

ISSCC 2022 • Thursday February 24th

8:00 AM	**Short Course:** High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics	**F3:** The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing and Imaging	**F4:** Paving the Way to 200Gb/s Transceivers	**F5:** How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms	**F6:** Computer Systems Under Attack – Paying the Performance Price for Protection

EE5: Shifting Tides of Innovation – Where is Cutting-Edge Research Happening Today?

Organizers: **Alicia Klinefelter**, *NVIDIA, Durham, NC*
Mingoo Seok, *Columbia University, New York, NY*

Co-Organizers: **Sophia Shao**, *University of California, Berkeley, CA*
Chiraag Juvekar, *Analog Devices, Cambridge, MA*

Moderator: **Vivek De,** *Intel, Hillsboro, OR*

As research becomes more complex, multidisciplinary and system oriented, the focal point of innovation has begun to shift. Resource constraints such as people per project or the cost of working in the latest technology node also impacts who can participate in cutting-edge research. Industry does not have strong incentives to publish their most innovative and competitive work, leaving many in the dark as to what the state of the art is within companies. Even within industry, innovation can come from research, product, or startups. On the academic side, funding bodies and trends can also impact the innovation process. How can we close this gap and who really has the edge? Is industry-guided academic research the way to get the best of both worlds? The traditional debate has been between academia and industry, but there are many more facets to the discussion. This panel explores a variety of perspectives of how innovation occurs across the industry.

Panelists:
James Myers, *Arm, Cambridge, United Kingdom*
Tezaswi Raja, *NVIDIA, Santa Clara, CA*
Nam Sung Kim, *University of Illinois, Urbana-Champaign, IL*
Scott Hanson, *Ambiq, Austin, TX*
Christal Gordon, *Booz Allen Hamilton, McLean, VA*
Thomas Parry, *SystematIC Design, Rotterdam, The Netherlands*

EE6: Next Trillion-Dollar Market

Co-Organizers: **Jane Gu,** *University of California, Davis, Davis, CA*
Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsin-Chu, Taiwan*
Kazuko Nishimura, *Panasonic, Moriguchi, Japan*
Patrick Mercier, *University of California, San Diego, La Jolla, CA*

Moderator: **Tom Lee**, *Stanford University, Stanford, CA*

Innovations and technologies, which impact humanity in many aspects, enable rapidly evolving and emerging applications: including 5G and beyond wireless communications, wireline communications, autonomous vehicle, sensing, artificial intelligence (AI), machine learning, internet of things (IoT), internet of everything (IoE), virtual reality (VR), augmented reality (AR), silicon photonics, quantum computing, etc. Which of these will be the next trillion-dollar market driver for chips?

A collection of distinguished experts, from various domains, had been assembled to discuss the challenges and opportunities for growth in multiple, potentially large, sectors; the enabling technologies in each sector; and the ones required, particularly, from the semiconductor industry, as well as their timelines and questions raised by **you**, the audience.

Panelists:
Lawrence Loh, *Mediatek, Hsinchu City, Taiwan*
Vladimir Stojanovic, *University of California, Berkeley, Berkeley, CA*
Hayato Wakabayashi, *Sony Semiconductor Solutions, Atsugi, Japan*
Nancy Shemwell, *Trilogy Networks, Dallas, TX*
Bill Dally, *NVIDIA, Incline Village, NV*
Jay Gambetta, *IBM Quantum, Yorktown Heights, NY*

Highlighted Chip Releases: Digital/ML

Session Chair: Dennis Sylvester, *University of Michigan, Ann Arbor, MI*
Session Co-Chair: *Thomas Burd, AMD, Santa Clara, CA*

10:15 AM

21.1 SambaNova SN10 RDU: A 7nm Dataflow Architecture to Accelerate Software 2.0
R. Prabhakar, S. Jairath, J. L. Shin
SambaNova Systems, Palo Alto, CA

10:45 AM

21.2 A64FX: 52-Core Processor Designed for the 442PetaFLOPS Supercomputer Fugaku
S. Yamamura, Y. Akizuki, H. Sekiguchi, T. Maruyama, T. Sano, H. Miyazaki, T. Yoshida
Fujitsu, Kawasaki, Japan

11:15 AM

21.3 Bonanza Mine: An Ultra-Low-Voltage Energy-Efficient Bitcoin Mining ASIC
V. B. Suresh[1], C. S. Katta[2], S. Rajagopalan[2], T. Z. Zhou[3], A. Patel[2], R. Rakha[2], N. K. Gopalakrishna[2], S. Mathew[1], A. Hukkoo[2]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA
[3]Intel, San Diego, CA

11:45 AM

21.4 The Wormhole AI Training Processor
D. Ignjatovic, D. W. Bailey, L. Bajic
Tenstorrent, Toronto, Canada

Conclusion 12:15 PM

Cryo-Circuits and Ultra-Low-Power Intelligent IoT

Session Chair: Sudip Shekhar, *University of British Columbia, Vancouver, Canada*
Session Co-Chair: Radu Berdan, *Kioxia, Tokyo, Japan*

8:30 AM

22.1 A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology

D. J. Frank[1], S. Chakraborty[1], K. Tien[1], P. Rosno[2], T. Fox[1], M. Yeck[1], J. A. Glick[1], R. Robertazzi[1], R. Richetta[2], J. F. Bulzacchelli[1], D. Ramirez[2], D. Yilma[2], A. Davies[2], R. V. Joshi[1], S. D. Chambers[2], S. Lekuch[1], K. Inoue[1], D. Underwood[1], D. Wisnieff[1], C. Baks[1], D. Bethune[3], J. Timmerwilke[1], B. R. Johnson[1], B. P. Gaucher[1], D. J. Friedman[1]

[1]IBM T. J. Watson Research Center, Yorktown Heights, NY
[2]IBM Systems, Rochester, MN; [3]IBM Almaden Research Center, San Jose, CA

9:00 AM

22.2 A Cryo-CMOS Controller IC with Fully Integrated Frequency Generators for Superconducting Qubits

K. Kang, D. Minn*, S. Bae, J. Lee, S. Bae, G. Jung, S. Kang, M. Lee, H-J. Song, J-Y. Sim*

*Equally-Credited Authors (ECAs), Pohang University of Science and Technology, Pohang, Korea

9:30 AM

22.3 A Cryogenic SiGe BiCMOS Hybrid Class B/C Mode-Switching VCO Achieving 201dBc/Hz Figure-of-Merit and 4.2GHz Frequency Tuning Range

Y. Peng[1,2], A. Ruffino[1], J. Benserhir[1], E. Charbon[1]

[1]Ecole Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland
[2]Southern University of Science and Technology, Shenzhen, China

Break 10:00 AM

10:15 AM

22.4 A WiFi and Bluetooth Backscattering Combo Chip Featuring Beam Steering via a Fully-Reflective Phased-Controlled Multi-Antenna Termination Technique Enabling Operation Over 56 Meters

S-K. Kuo, M. Dunna, D. Bharadia, P. P. Mercier, University of California, San Diego, CA

10:45 AM

22.5 A 108nW 0.8mm² Analog Voice Activity Detector (VAD) Featuring a Time-Domain CNN as a Programmable Feature Extractor and a Sparsity-Aware Computational Scheme in 28nm CMOS

F. Chen[1], K-F. Un[1], W-H. Yu[1], P-I. Mak[1], R. P. Martins[1,2]

[1]University of Macau, Macau, China
[2]University of Lisboa, Lisbon, Portugal

11:15 AM

22.6 A 23µW Solar-Powered Keyword-Spotting ASIC with Ring-Oscillator-Based Time-Domain Feature Extraction

K. Kim[1], C. Gao[1], R. Graça[1], I. Kiselev[1], H-J. Yoo[2], T. Delbruck[1], S-C. Liu[1]

[1]University of Zurich and ETH Zurich, Zurich, Switzerland
[2]KAIST, Daejeon, Korea

11:45 AM

22.7 An 82nW 0.53pJ/SOP Clock-Free Spiking Neural Network with 40µs Latency for AIoT Wake-Up Functions Using Ultimate-Event-Driven Bionic Architecture and Computing-in-Memory Technique

Y. Liu[1], Z. Wang[1,2], W. He[1], L. Shen[1], Y. Zhang[1], P. Chen[1], M. Wu[1], H. Zhang[1], P. Zhou[3], J. Liu[3], G. Sun[1], J. Ru[1], L. Ye[1,2], R. Huang[1]

[1]Peking University, Beijing, China
[2]Advanced Institute of Information Technology of Peking University, Hangzhou, China
[3]Nano Core Chip Electronic Technology, Hangzhou, China

Conclusion 12:15 PM

Frequency Synthesizers

Session Chair: Jun Yin, *University of Macau, Taipa, Macau*
Session Co-Chair: Jeremy Dunworth, *Qualcomm Technologies, La Jolla, CA*

8:30 AM

23.1 A Cascaded PLL (LC-PLL + RO-PLL) with a Programmable Double Realignment Achieving 204fs Integrated Jitter (100kHz to 100MHz) and -72dB Reference Spur

T-H. Tsai[1], R-B. Sheen[1], S-Y. Hsu[1], Y-T. Chang[1], C-H. Chang[1], R. B. Staszewski[2]
[1]TSMC, Hsinchu, Taiwan
[2]University College Dublin, Dublin, Ireland

9:00 AM

23.2 A 188fs$_{rms}$-Jitter and –243dB-FoM$_{jitter}$ 5.2GHz-Ring-DCO-Based Fractional-N Digital PLL with a 1/8 DTC-Range-Reduction Technique Using a Quadruple-Timing-Margin Phase Selector

C. Hwang, H. Park*, T. Seong, J. Choi*
*Equally-Credited Authors (ECAs), KAIST, Daejeon, Korea

9:30 AM

23.3 A 2.6-to-4.1GHz Fractional-N Digital PLL Based on a Time-Mode Arithmetic Unit Achieving -249.4dB FoM and -59dBc Fractional Spurs

Z. Gao[1], J. He[1], M. Fritz[2], J. Gong[1], Y. Shen[1], Z. Zong[1], P. Chen[3], G. Spalink[2], B. Eitel[2], K. Yamamoto[4], R. B. Staszewski[1,3], M. S. Alavi[1], M. Babaie[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Sony Europe, Stuttgart, Germany
[3]University College Dublin, Dublin, Ireland
[4]Sony Semiconductor Solutions, Atsugi, Japan

Break 10:00 AM

10:15 AM

23.4 A 100MHz-Reference, 8GHz/16GHz, 177fs$_{rms}$/223fs$_{rms}$ RO-Based IL-ADPLL Incorporating Reference Octupler with Probability-Based Fast Phase-Error Calibration

H. Kim[1], H-S. Oh[2], W. Jung[1], Y. Song[1], J. Oh[3], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea
[2]University of California, Berkeley, CA
[3]Columbia University, New York, NY

10:45 AM

23.5 A Sub-100MHz Reference-Driven 25-to-28GHz Fractional-N PLL with -250dB FoM

D. Yang[1], D. Murphy[1], H. Darabi[1], A. Behzad[1], A. Abidi[2], S. Au[1], S. Mundlapudi[1], K. Shi[1], W. Leng[2]
[1]Broadcom, San Jose, CA
[2]University of California, Los Angeles, CA

11:15 AM

23.6 A 68.6fs$_{rms}$-Total-Integrated-Jitter and 1.56µs-Locking-Time Fractional-N Bang-Bang PLL Based on Type-II Gear Shifting and Adaptive Frequency Switching

S. M. Dartizio[1], F. Buccoleri*[1], F. Tesolin[1], L. Avallone[2], A. Santiccioli[1], A. Iesurum[3], G. Steffan[2], D. Cherniak[2], L. Bertulessi[1], A. Bevilacqua[3], C. Samori[1], A. L. Lacaita[1], S. Levantino[1]*
*Equally-Credited Authors (ECAs)
[1]Politecnico di Milano, Milan, Italy; [2]Infineon Technologies, Villach, Austria
[3]University of Padova, Padova, Italy

11:45 AM

23.7 A 25.8GHz Integer-N PLL with Time-Amplifying Phase-Frequency Detector Achieving 60fs$_{rms}$ Jitter, -252.8dB FoM$_J$, and Robust Lock Acquisition Performance

X. Geng, Y. Tian, Y. Xiao, Z. Ye, Q. Xie, Z. Wang
University of Electronic Science and Technology of China, Chengdu, China

Conclusion 12:15 PM

Low-Power and UWB Radios for Communication and Ranging

Session Chair: Maryam Tabesh, *Google, Mountain View, CA*
Session Co-Chair:
Jan Prummel, *Dialog Semiconductor B.V., A Renesas Company, 's-Hertogenbosch, The Netherlands*

8:30 AM

24.1 A Long-Range Narrowband RF Localization System with a Crystal-Less Frequency-Hopping Receiver

C-W. Tseng[1], D. Komma[1], K-Y. Chen[1], R. Rothe[1], Z. Feng[1], M. Yasuda[2], M. Kawaminami[3], H-S. Kim[1], D. Blaauw[1]
[1]University of Michigan, Ann Arbor, MI
[2]United Semiconductor Japan, Kuwana, Japan; [3]United Semiconductor Japan, Yokohama, Japan

9:00 AM

24.2 A 1.66Gb/s and 5.8pJ/b Transcutaneous IR-UWB Telemetry System with Hybrid Impulse Modulation for Intracortical Brain-Computer Interfaces

M. Song[1], Y. Huang[1,2], Y. Shen[1], C. Shi[1,3], A. Breeschoten[1], M. Konijnenburg[1], H. Visser[1], J. Romme[1], B. Dutta[4], M. S. Alavi[2], C. Bachmann[1], Y-H. Liu[1]
[1]imec-Netherlands, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
[3]Eindhoven University of Technology, Eindhoven, The Netherlands; [4]imec, Leuven, Belgium

9:30 AM

24.3 A 6.5-to-10GHz IEEE 802.15.4/4z-Compliant 1T3R UWB Transceiver

R. Chen, Y. Xiao, Y. Chen, H. Xu, P. Yu, Q. Peng, X. Li, X. Guo, J. Huang, N. Li, X. Hu, R. Ou, W. Liu, B. Chen, W. Zhang, X. Xin, B. Zhao, Z. Chen
Newradio Technology, Shenzhen, China

Break 10:00 AM

10:15 AM

24.4 A 22nm 0.84mm² BLE Transceiver with Self IQ-Phase Correction Achieving 39dB Image Rejection and On-Chip Antenna Impedance Tuning

K. Shibata, H. Matsui, H. Asano, Y. Kusaka, K. Ueda, N. Matsuno, H. Sato
Renesas Electronics, Tokyo, Japan

10:45 AM

24.5 A 266μW Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive Balun-LNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77dB SFDR and -3dBm OOB-B_{-1dB}

H. Shao[1], P-I. Mak[1], G. Qi[2], R. P. Martins[1,3]
[1]University of Macau, Macau, China
[2]Sun Yat-Sen University, Zhuhai, China
[3]University of Lisboa, Lisbon, Portugal

11:15 AM

24.6 A 110μW 2.5kb/s -103dBm-Sensitivity Dual-Chirp Modulated ULP Receiver Achieving -41dB SIR

M. Moosavifar, J. Im*, T. Odelberg, D. Wentzloff*
*Equally-Credited Authors (ECAs)
University of Michigan, Ann Arbor, MI

11:45 AM

24.7 An LPWAN Radio with a Reconfigurable Data/Duty-Cycled-Wake-Up Receiver

K-M. Kim[1], K-S. Choi[1], H. Jung[1,2], B. Yun[1], S. Kim[2], W. Oh[2], E-S. Lee[3], S. Park[2], E-R. Jeong[3], J. Ko[2], S-G. Lee[1]
[1]KAIST, Daejeon, Korea; [2]PHYCHIPS, Daejeon, Korea
[3]Hanbat National University, Daejeon, Korea

Conclusion 12:15 PM

Noise-Shaping ADCs

Session Chair: ***Dominique Morche,*** *CEA-LETI, Grenoble, France*
Session Co-Chair: ***Yan Zhu,*** *University of Macau, Taipa, Macau*

8:30 AM

25.1 A 4.4μW 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-Based ADC with Pseudo Virtual Ground Feedforward Linearization

C. Pochet, D. Hall
University of California, San Diego, CA

9:00 AM

25.2 A 2.87μW 1kHz-BW 94.0dB-SNDR 2-0 MASH ADC using FIA with Dynamic-Body-Biasing Assisted CLS Technique

Y. Hu[1], Y. Zhao[1], W. Qu[1], L. Ye[2], M. Zhao[1], Z. Tan[1]
[1]Zhejiang University, Hangzhou, China
[2]Peking University, Beijing, China

9:30 AM

25.3 A 0.0375mm² 203.5μW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS

C. Y. Lee, U-K. Moon
Oregon State University, Corvallis, OR

Break 10:00 AM

10:15 AM

25.4 A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH ΔΣ ADC in 40nm CMOS

Q. Liu[1,2], L. Breems[1,2], C. Zhang[1,2], S. Bajoria[1,2], M. Bolatkale[2,3], R. Rutten[2], G. Radulov[1]
[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands
[3]Delft University of Technology, Delft, The Netherlands

10:45 AM

25.5 A 28nm 6GHz 2b Continuous-Time ΔΣ ADC with -101dBc THD and 120MHz Bandwidth Using Digital DAC Error Correction

M. Bolatkale[1], R. Rutten[1], H. Brekelmans[1], S. Bajoria[1], Y. Gao[1], B. Burdiek[2], L. Breems[1]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]NXP Semiconductors, Hamburg, Germany

11:15 AM

25.6 An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique

T. Wang, T. Xie, Z. Liu, S. Li
Georgia Institute of Technology, Atlanta, GA

Conclusion 11:45 PM

Highlighted Chip Releases: Systems and Quantum Computing

Session Chair: Fabio Sebastiano, *Delft University of Technology, Delft, The Netherlands*
Session Co-Chair: *Alice Wang, Everactive, Plano, TX*

1:30 PM

26.1 Beyond-Classical Computing Using Superconducting Quantum Processors

J. Bardin[1,2]
[1]Google Quantum AI, Goleta, CA
[2]University of Massachusetts, Amherst, MA

2:00 PM

26.2 Design Considerations for Superconducting Quantum Systems

G. Zettles[1], S. Willenborg[1], B. Johnson[2], A. Wack[2], B. Allison[1]
[1]IBM, Rochester, MN
[2]IBM, Yorktown Heights, NY

2:30 PM

26.3 Augmented Reality – The Next Frontier of Image Sensors and Compute Systems

C. Liu, S. Chen, T-H. Tsai, B. De Salvo, J. Gomez
Meta Reality Labs, Redmond, WA

3:00 PM

26.4 3D V-Cache: The Implementation of a Hybrid-Bonded 64MB Stacked Cache for a 7nm x86-64 CPU

J. Wuu[1], R. Agarwal[2], M. Ciraula[1], C. Dietz[1], B. Johnson[1], D. Johnson[1], R. Schreiber[3], R. Swaminathan[3], W. Walker[1], S. Naffziger[1]
[1]AMD, Fort Collins, CO
[2]AMD, Santa Clara, CA
[3]AMD, Austin, TX

Break 3:30 PM

mm-Wave & Sub-6GHz Receivers and Transceivers for 5G Radios

Session Chair: Shahriar Shahramian, *Nokia – Bell Labs, New Providence, NJ*
Session Co-Chair: Byung-Wook Min, *Yonsei University, Seoul, Korea*

3:45 PM

27.1 A 16-Channel, 28/39GHz Dual-Polarized 5G FR2 Phased-Array Transceiver IC with a Quad-Stream IF Transceiver Supporting Non-Contiguous Carrier Aggregation up to 1.6GHz BW

A. Verma[1], V. Bhagavatula[1], A. Singh[1], W. Wu[1], H. Nagarajan[1], P-K. Lau[1], X. Yu[1], O. Elsayed[1], A. Jain[1], A. Sarkar[1], F. Zhang[1], C-C. Kuo[1], P. McElwee[1], P-Y. Chiang[1], C. Guo[1], Z. Bai[1], T. Chang[1], A. Mann[1], A. Rydin[1], X. Zhao[1], J. Lee[2], D. Yoon[2], C-W. Yao[1], S. I. Lu[1], S. W. Son[1], T. B. Cho[2]
[1]Samsung Semiconductor, San Jose, CA
[2]Samsung Electronics, Hwaseong, Korea

4:15 PM

27.2 A Power-Efficient 24-to-71GHz CMOS Phased-Array Receiver Utilizing Harmonic-Selection Technique Supporting 36dB Inter-Band Blocker Rejection for 5G NR

J. Pang, Y. Zhang, Z. Li, M. Tang, Y. Liao, A. A. Fadila, A. Shirane, K. Okada
Tokyo Institute of Technology, Tokyo, Japan

4:45 PM

27.3 A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams

B. Sadhu[1], A. Paidimarri[1], W. Lee[1], M. Yeck[1], C. Ozdag[1], Y. Tojo[2], J-O. Plouchart[1], X. Gu[1], Y. Uemichi[2], S. Chakraborty[1], Y. Yamaguchi[2], N. Guan[2], A. Valdes-Garcia[1]
[1]IBM T. J. Watson Research Center, Yorktown Heights, NY
[2]Fujikura, Sakura, Japan

5:00 PM

27.4 A Hybrid Coupler-First 5GHz Noise-Cancelling Dual-Mode Receiver with +10dBm In-Band IIP3 in Current-Mode and 1.7dB NF in Voltage-Mode

K. Yang, C. C. Boon, Z. Liu, J. Piao, T. Guo, Y. Dong, C. Li, A. Zhou, Z. Yang, X. Wang, Y. Liu
Nanyang Technological University, Singapore, Singapore

5:15 PM

27.5 A Single-Path Digital-IF Receiver Supporting Inter/Intra 5-CA with a Single Integer LO-PLL in 14nm CMOS FinFET

B. Sung, H-G. Seok, J. Kim, J. Lee, T. Jang, I. Jang, Y. Kim, A. Yu, J-H. Jang, J. Lee, J. Bae, E. Park, S. Lee, S. Lee, J. Kim, B. Kim, Y. Lim, S. Oh, J. Lee, B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

Conclusion 5:45 PM

DRAM and Interface

Session Chair: Bor-Doou Rong, *Etron, Hsinchu, Taiwan*
Session Co-Chair: Hye-Ran Kim, *Samsung Electronics, Hwasung, Korea*

1:30 PM

28.1 A 192Gb 12-High 896GB/s HBM3 DRAM with a TSV Auto-Calibration Scheme and Machine-Learning Based Layout Optimization

M-J. Park, H. S. Cho, T-S. Yun, S. Byeon, Y. J. Koo, S. Yoon, D. U. Lee, S. Choi, J. Park, J. Lee, K. Cho, J. Moon, B-K. Yoon, Y-J. Park, S-M. Oh, C. K. Lee, T-K. Kim, S-H. Lee, H-W. Kim, Y. Ju, S-K. Lim, S. G. Baek, K. Y. Lee, S. H. Lee, W. S. We, S. Kim, Y. Choi, S-H. Lee, S. M. Yang, G. Lee, I-K. Kim, Y. Jeon, J-H. Park, J. C. Yun, C. Park, S-Y. Kim, S. Kim, D-Y. Lee, S-H. Oh, T. Hwang, J. Shin, Y. Lee, H. Kim, J. Lee, Y. Hur, S. Lee, J. Jang, J. Chun, J. Cho
SK hynix, Icheon, Korea

2:00 PM

28.2 A 16Gb 27Gb/s/pin T-coil based GDDR6 DRAM with Merged-MUX TX, Optimized WCK Operation, and Alternative-Data-Bus

D. Lee, H-J. Kwon, D. Kwon, J. Baek, C. Cho, S. Kim, D. An, C. Chang, U. Lim, J. Im, W. Sung, H-R. Kim, S-Y. Park, H. Kim, H. Seol, J. Kim, J. Shin, K-Y. Kang, Y-H. Kim, S. Kim, W. Park, S-J. Kim, C. Lee, S. Lee, T. Park, C. Oh, H. Ban, H. Ko, H. Song, T-Y. Oh, S. Hwang, K. S. Oh, J. Choi, J. Lee
Samsung Electronics, Hwaseong, Korea

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28.3 A 16Gbit 9.5Gb/s/pin LPDDR5X SDRAM with Low-Power Schemes Exploiting Dynamic Voltage Frequency Scaling and Offset-Calibrated Readout Sense Amplifiers in a Fourth Generation 10nm DRAM Process

D-H. Kim, B. Song, H-A. Ahn, W. Ko, S. Do, S. Cho, K. Kim, S-H. Oh, H-Y. Joo, G. Park, J-H. Jang, Y-H. Kim, D. Lee, J. Jung, Y. Kwon, Y. Kim, J. Jung, S. O, S. Lee, J. Lim, J. Son, J. Min, H. Do, J. Yoon, I. Hwang, J. Park, H. Shim, S. Yoon, D. Choi, J. Lee, S. Woo, E. Hong, J. Choi, J-S. Kim, S. Han, J. Bang, B. Park, J. Kim, S-K. Choi, G-H. Han, Y-C. Sung, W-I. Bae, J-D. Lim, S. Lee, C. Yoo, S. J. Hwang, J. Lee
Samsung Electronics, Hwaseong, Korea

3:00 PM

28.4 A 20 Gb/s/pin 1.18pJ/b 1149um² Single-Ended Inverter-based 4-tap Addition-Only Feed-Forward Equalization Transmitter With Improved Robustness to Coefficient Errors in 28 nm CMOS

C. Moon, J. Seo, M. Lee, I. Jang, B. Kim, Pohang University of Science and Technology, Pohang, Korea

Break 3:30 PM

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28.5 A 0.385pJ/bit 10Gb/s TIA-terminated Di-code Transceiver with Edge-delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces

H. Park[1], Y. Choi[1], J. Sim[1], J. Choi[1], Y. Kwon[1], J. Song[2], C. Kim[1]
[1]Korea University, Seoul, Korea; [2]Incheon National University, Incheon, Korea

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28.6 A 78.8fJ/bit/mm 12.0Gb/s/Wire Capacitively Driven On-Chip Link Over 5.6mm with an FFE-Combined Ground-Forcing Biasing Technique for DRAM Global Bus Line in 65nm CMOS

S. Lee, J. Yun, S. Kim, Seoul National University, Seoul, Korea

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28.7 A 20 Gb/s/pin 0.0024 mm² Single-Ended DECS TRX with CDR-less Self-Slicing/Auto-Deserialization to Improve Tolerance on Duty Cycle Error and RX Supply Noise for DCC/CDR-less Short-Reach Memory Interfaces

J. Seo[1], S. Lee[2], M. Lee[1], C. Moon[1], B. Kim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

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28.8 A 2nd-order Adaptive Filter-based Supply Noise Induced Jitter Cancelling Clock Distribution Network for LPDDR5 Mobile DRAM

Y. Jung[1], S. Lee*[2], H. Kim[3], S. Cho[4]*, *Equally-Credited Authors (ECAs)
[1]Samsung Electronics, Hwaseong-si, Korea; [2]SK hynix, Icheon, Korea
[3]Korea Aerospace Research Institute, Daejeon, Korea; [4]KAIST, Daejeon, Korea

Conclusion 5:15 PM

ML Chips for Emerging Applications

Session Chair: Jun Deguchi, *Kioxia, Kawasaki, Japan*
Session Co-Chair: Jae-sun Seo, *Arizona State University, Tempe, AZ*

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29.1 184QPS/W 64Mb/mm² 3D Logic-to-DRAM Hybrid Bonding with Process-Near-Memory Engine for Recommendation System

D. Niu[1], S. Li[1], Y. Wang[1], W. Han[1], Z. Zhang[2], Y. Guan[2], T. Guan[3], F. Sun[1], F. Xue[1], L. Duan[1], Y. Fang[1], H. Zheng[1], X. Jiang[4], S. Wang[4], F. Zuo[4], Y. Wang[4], B. Yu[4], Q. Ren[4], Y. Xie[1]
[1]Alibaba DAMO Academy, Sunnyvale, CA
[2]Alibaba DAMO Academy, Beijing, China
[3]Alibaba DAMO Academy, Shanghai, China
[4]UniIC, Xian, China

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29.2 A 28nm 27.5TOPS/W Approximate-Computing-Based Transformer Processor with Asymptotic Sparsity Speculating and Out-of-Order Computing

Y. Wang[1], Y. Qin[1], D. Deng[1], J. Wei[1], Y. Zhou[1], Y. Fan[1], T. Chen[2], H. Sun[1], L. Liu[1], S. Wei[1], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]Tsing Micro, Beijing, China

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29.3 A 28nm 15.59μJ/Token Full-Digital Bitline-Transpose CIM-Based Sparse Transformer Accelerator with Pipeline/Parallel Reconfigurable Modes

F. Tu[1,2], Z. Wu[1], Y. Wang[1], L. Liang[2], L. Liu[2], Y. Ding[2], L. Liu[1], S. Wei[1], Y. Xie[2], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]University of California, Santa Barbara, CA

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29.4 ReckOn: A 28nm Sub-mm² Task-Agnostic Spiking Recurrent Neural Network Processor Enabling On-Chip Learning over Second-Long Timescales

C. Frenkel, G. Indiveri
University of Zurich and ETH Zurich, Zurich, Switzerland

Break 3:30 PM

Power Management Techniques

Session Chair: Min Chen, *Analog Devices, Santa Clara, CA*
Session Co-Chair: Li Geng, *Xi'an Jiaotong University, Xi'an, China*

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30.1 A 32nA Fully Autonomous Multi-Input Single-Inductor Multi-Output Energy Harvesting and Power Management Platform with 1.2×10^5 Dynamic Range, Integrated MPPT, and Multi-Modal Cold Start-Up

S. Li, X. Liu, B. H. Calhoun
University of Virginia, Charlottesville, VA

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30.2 A 130V Triboelectric Energy-Harvesting Interface in 180nm BCD with Scalable Multi-Chip-Stacked Bias-Flip and Daisy-Chained Synchronous Signaling Technique

J. Lee, S-H. Lee, G-G. Kang, J-H. Kim, G-H. Cho, H-S. Kim
KAIST, Daejeon, Korea

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30.3 A Reconfigurable Series-Parallel Charger for Dual-Battery Applications with 89W 97.7% Efficiency in Direct Charging Mode

S. Lee, T. Jeong, Y. Cho, J. Yoo, S. Cho, M. Kwon, D. Cho, S. H. Kang, J. W. Heo, H-S. Oh, S. U. Kwak
Samsung Electronics, Hwaseong, Korea

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30.4 A 0.76V V_{in} Triode Region 4A Analog LDO with Distributed Gain Enhancement and Dynamic Load-Current Tracking in Intel 4 CMOS Featuring Active Feedforward Ripple Shaping and On-Chip Power Noise Analyzer

X. Liu, H. Krishnamurthy, R. Liu, K. Ravichandran, Z. Ahmed, N. Desai, N. Butzen, J. Tschanz, V. De
Intel, Portland, OR

Conclusion 5:45 PM

Audio Amplifiers

Session Chair: Qinwen Fan, *Delft University of Technology, Delft, The Netherlands*
Session Co-Chair: Mahdi Kashmiri, *Broadcom, San Jose, CA*

1:30 PM

31.1 A -117dBc THD (-132dBc HD3) and 126dB DR Audio Decoder with Code-Change-Insensitive RT-DEM Algorithm and Circuit Technique for Relaxing Velocity Saturation Effect of Poly Resistors

S-H. Wen, C-H. Hsiao, S-H. Chien, Y-C. Chen, K-H. Chen, K-D. Chen
MediaTek, Hsinchu, Taiwan

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31.2 A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier

H. Zhang[1], M. Berkhout[2], K. A. A. Makinwa[1], Q. Fan[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands

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31.3 A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM

W-H. Sun, S-H. Chien, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

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31.4 A -91dB THD+N Resistor-Less Class-D Piezoelectric Speaker Driver Using a Dual Voltage/ Current Feedback for LC Resonance Damping

S. Karmakar[1], M. Berkhout [2], K. A. A. Makinwa[1], Q. Fan[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands

Break 3:30 PM

Ultrasound and Beamforming Applications

Session Chair: Jun-Chau Chien, *National Taiwan University, Taipei, Taiwan*
Session Co-Chair: Jerald Yoo, *National University of Singapore, Singapore, Singapore*

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32.1 BatDrone: A 9.83M-focal-points/s 7.76µs-Latency Ultrasound Imaging System with On-Chip Per-Voxel RX Beamfocusing for 7m-Range Drone Applications

L. Wu[1], J. Guo*[1], R. Jiang[1], Y. Peng[2], H. Wu[1], J. Li[1], Y. Dong[1], M. Zhang[1], Z. Li[1], K. A. Ng[3], C-W. Tsai[1], L. Zhang[1], L. Lin[4], L. Lin[2], J. Yoo[1,5]*
*Equally-Credited Authors (ECAs)
[1]National University of Singapore, Singapore, Singapore
[2]University of California, Berkeley, CA
[3]Digipen Institute of Technology, Singapore, Singapore
[4]Southern University of Science and Technology, Shenzhen, China
[5]The N.1 Institute for Health, Singapore, Singapore

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32.2 A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes

Y. Hopf[1], B. Ossenkoppele[1], M. Soozande[2], E. Noothout[1], Z-Y. Chang[1], C. Chen[1], H. Vos[1,2], H. Bosch[2], M. Verweij[1,2], N. de Jong[1,2], M. Pertijs[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Erasmus MC, Rotterdam, The Netherlands

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32.3 A 1.2mW/channel 100µm-Pitch-Matched Transceiver ASIC with Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3D Ultrasound Imaging

P. Guo[1], F. Fool[1], E. Noothout[1], Z-Y. Chang[1], H. J. Vos[1,2], J. G. Bosch[2], M. D. Verweij[1,2], N. de Jong[1,2], M. A. P. Pertijs[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Erasmus MC, Rotterdam, The Netherlands

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32.4 An Electronically Tunable Multi-Frequency Air-Coupled CMUT Receiver Array with sub-100µPa Minimum Detectable Pressure Achieving a 28kb/s Wireless Uplink Across a Water-Air Interface

A. Singhvi, A. Fitzpatrick, A. Arbabian
Stanford University, Stanford, CA

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32.5 A Multimode 157µW 4-Channel 80dBA-SNDR Speech-Recognition Frontend with Self-DOA Correction Adaptive Beamformer

T. Kang[1], S. Lee*[1], S. Song[1], M. R. Haghighat[2], M. P. Flynn[1]*
*Equally-Credited Authors (ECAs)
[1]University of Michigan, Ann Arbor, MI
[2]Intel, Santa Clara, CA

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Domain-Specific Processors

Session Chair: Sanu Mathew, *Intel, Portland, OR*
Session Co-Chair: Chia-Hsiang Yang, *National Taiwan University, Taipei, Taiwan*

1:30 PM

33.1 A 1.05A/m Minimum Magnetic Field Strength Single-Chip Fully Integrated Biometric Smart Card SoC Achieving 1014.7ms Transaction Time with Anti-Spoofing Fingerprint Authentication

J-S. Chang, E. Jang, Y. Choi, M. Song, S. Lee, G-J. Kang, J. Kim, S-W. Kang, U. Song, C-Y. Cho, J. Lee, K. Seo, S. Song, S. U. Kwak
Samsung Electronics, Hwaseong, Korea

2:00 PM

33.2 A 96.2nJ/class Neural Signal Processor with Adaptable Intelligence for Seizure Prediction

Y-Y. Hsieh, Y-C. Lin, C-H. Yang
National Taiwan University, Taipei, Taiwan

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33.3 A HD 31fps 7×7-View Light-Field Factorization Processor for Dual-Layer 3D Factored Display

L-Q. Weng, L-D. Chen, H-C. Cheng, A-Y. Zheng, K-P. Lin, C-T. Huang
National Tsing Hua University, Hsinchu, Taiwan

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33.4 DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms

D. Im, G. Park, Z. Li, J. Ryu, S. Kang, D. Han, J. Lee, H-J. Yoo
KAIST, Daejeon, Korea

Break 3:30 PM

Hardware Security

Session Chair: Chiraag Juvekar, *Analog Devices, Boston, MA*
Session Co-Chair: Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*

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34.1 A 28nm 48KOPS 3.4µJ/Op Agile Crypto-Processor for Post-Quantum Cryptography on Multi-Mathematical Problems

Y. Zhu[1], W. Zhu[1], M. Zhu[2], C. Li[1], C. Deng[1], C. Chen[1], S. Yin[1], S. Yin[1], S. Wei[1], L. Liu[1]
[1]Tsinghua University, Beijing, China
[2]Micro Innovation Integrated Circuit Design, Wuxi, China

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34.2 Side-Channel Attack Counteraction via Machine Learning-Targeted Power Compensation for Post-Silicon HW Security Patching

Q. Fang[*1], L. Lin*[*1,2], Y. Z. Wong[1], H. Zhang[1], M. Alioto[1]*
*Equally-Credited Authors (ECAs)
[1]National University of Singapore, Singapore, Singapore
[2]Southern University of Science and Technology, Shenzhen, China

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34.3 ShieldNN: A Threshold-Implementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks

S. Maji[1], U. Banerjee[2], S. H. Fuller[1,3], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Indian Institute of Science, Bengaluru, India
[3]Analog Devices, Wilmington, MA

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34.4 An 8.3-to-18Gbps Reconfigurable SCA-Resistant/Dual-Core/Blind-Bulk AES Engine in Intel 4 CMOS

R. Kumar, V. B. Suresh, M. A. Anders, S. K. Hsu, A. Agarwal, V. K. De, S. K. Mathew
Intel, Hillsboro, OR

Conclusion 5:45 PM

Short Course: High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair, ***Daniel Friedman*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications** ***Boris Murmann,*** *Stanford University, Stanford, CA*
10:00 AM	Break
10:30 AM	**Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations** ***Gabriele Manganaro,*** *MediaTek, Woburn, MA*
12:15 PM	Lunch
1:20 PM	**High-Precision and Low-Power ADCs** ***Pieter Harpe,*** *Eindhoven University of Technology, Eindhoven, The Netherlands*
2:50 PM	Break
3:20 PM	**Emerging Data-Converter Concepts** ***Nan Sun****, Tsinghua University, Beijing, China*
4:50 PM	Conclusion

Introduction

Data converters provide the gateway between the analog and digital worlds. They play a critical role in a vast range of systems, and integrated converters represent a central and growing element in high performance designs in applications from wireline to wireless and more. In this course, we start with an introduction to data converters, discussing key topologies, metrics, and the associated trade space. We continue with a discussion of ultra-high data rate converter design approaches before moving to high precision and low power converter topics. In our final session, we discuss emerging data converter concepts that will shape the future of research in this area.

8:30 AM
SC1:
Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications

Boris Murmann, *Stanford University, Stanford, CA*

This presentation provides a short introduction to ADCs and DACs. The intent is to prepare the audience for the subsequent talks that will cover intricate details of modern, fine-tuned realizations. Topics include elementary data converter building blocks and their imperfections, converter topologies and their basic tradeoffs, performance metrics and figures of merit, as well as selected application aspects.

Boris Murmann is a Professor of Electrical Engineering at Stanford University. He joined Stanford in 2004 after completing his Ph.D. degree in electrical engineering at the University of California, Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Since 2004, he has worked as a consultant with numerous Silicon Valley companies. Dr. Murmann's research interests are in mixed-signal integrated circuit design, with special emphasis on sensor interfaces, data converters and embedded machine learning. He has served the Data Converter Subcommittee Chair and Technical Program Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He is a Fellow of the IEEE.

10:30 AM
SC2:
Ultra-High-Data-Rate ADCs and DACs: Architectures and Implementations

Gabriele Manganaro, *MediaTek, Woburn, MA*

Ten years ago or so, the term high-speed data converter was synonymous with sample rates on the order of a few hundreds of MHz, barring rare exceptions. Today, medium resolution ADCs (10-to-12b) and DACs clocked at tens of GHz, and even faster 6-to-8b converters, have been demonstrated without melting the die. So how could this level of advancement happen in the face of the end of Dennard scaling? The answer lies with the combination of architecture innovation and digital assistance. This presentation will give an overview of this rapidly (no pun intended) developing topic, aiming to illustrate the key design principles, their practical applicability, and will complement this material with examples of recently published multi-GSPS data converters.

Gabriele Manganaro (Fellow IEEE) holds a Dr. Eng. (1994) and a Ph.D. degree (1997) in Electronics from the University of Catania, Italy. He has worked in analog IC design, primarily in high-speed data converters design, both in Europe and the USA for over twenty years. He's presently a Director of Technology at MediaTek in Woburn, Massachusetts. He has authored/co-authored more than 60 peer-reviewed papers, three books (notably "Advanced Data Converters", Cambridge University Press, 2011) and has been granted 18 US patents, with more pending.

1:20 PM
SC3:
High-Precision and Low-Power ADCs

Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*

ADC designs are progressing rapidly over time in terms of architectural developments and circuit innovations. In this talk, we will focus on high-precision designs and on low-power design techniques of ADC topologies such as pipelined ADCs, Delta-Sigma modulators, and SAR (successive-approximation) ADCs. Besides discussing general challenges and solutions, some state-of-the-art ADC examples will be explained in the context of the principles outlined in this lecture, and a short review from a system integration perspective will be given.

Pieter Harpe received M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands. He spent several years as a researcher at imec, The Netherlands, and joined Eindhoven University of Technology in 2011, where he is currently Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly AACD workshop, an analog subcommittee chair for the ESSCIRC conference, and the SSCS CONFedu program chair. He served as an ISSCC ITPC member, SSCS Distinguished Lecturer, and JSSC guest editor. He is a Senior Member of the IEEE and a recipient of the ISSCC 2015 Distinguished Technical Paper Award.

3:20 PM
SC4:
Emerging Data-Converter Concepts

Nan Sun*, Tsinghua University, Beijing, China*

This talk presents several novel data-converter architectures, including hybrid ADCs that combine traditional architectures (e.g., a noise-shaping SAR) and Nyquist-rate ADCs with continuous-time (CT) front ends (e.g., a CT-pipe and CT-SAR). It also includes scaling-friendly time-domain ADCs that use digital gates to process analog signals. This talk also covers circuit-level innovations, including the use of open-loop and closed-loop dynamic amplifiers for residue amplification, as well as noise cancellation techniques that break the kT/C noise limit.

Nan Sun is a Professor of Electronic Engineering at Tsinghua University. He was Assistant and then Associate Professor with the University of Texas at Austin. He received B.Sc. degree from Tsinghua University and PhD degree from Harvard University. He received NSF Career Award in 2013, and IEEE SSCS New Frontier Award in 2020. He has graduated 24 PhDs (9 of whom are professors) and published 200 papers, including 30+ JSSC and 40+ ISSCC/VLSI/CICC papers. He serves on the TPC of CICC and A-SSCC. He served as an Associate Editor for IEEE TCAS-I and JSSC. He also serves as a Distinguished Lecturer for IEEE Circuits and Systems Society as well as IEEE Solid-State Circuits Society.

F3: The Path to 6G: Architectures, Circuits, Technologies for Sub-THz Communications, Sensing, and Imaging

Organizer: ***Giuseppe Gramegna,*** *IMEC, Leuven, Belgium*

Committee: ***Shuhei Amakawa,*** *Hiroshima University, Higashihiroshima, Japan*
Matteo Bassi, *Infineon Technologies, Villach, Austria*
Patrick Reynaert, *KU Leuven, Leuven, Belgium*
Swaminathan Sankaran, *Texas Instruments, Dallas, TX*
Ho-Jin Song, *Pohang University of Science and Technology, Pohang, Korea*

Champions: ***Andreia Cathelin,*** *STMicroelectronics, Crolles, France*
Kostas Doris, *NXP, Eindhoven, The Netherlands*
Chih-Ming Hung, *MediaTek, Taipei, Taiwan*

The demand for faster communications and wider coverage keeps fueling research towards 6G that will leverage higher frequencies within a broader application spectrum. This is stimulating rapid transformations and innovations in several fields, such as communication, sensing, and imaging. A wide range of new architectures, circuits and technologies are under investigation to support this trend. In this forum, eight experts will illuminate the way to the future by sharing their expertise in the fields of sub-THz communications, imaging, and sensing by transversally focusing on circuits, architectures, and also technology, packaging, and testing solutions.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Giuseppe Gramegna,*** *IMEC, Leuven, Belgium*
8:20 AM	**6G Communications: Vision and Challenges** ***Gary Xu*****,** *Samsung, Plano, TX*
9:05 AM	**Emerging Device and Heterogenous Integration Technologies for sub-THz Applications** ***Nadine Collaert*****,** *IMEC, Leuven, Belgium*
9:50 AM	Break
10:00 AM	**Highly Integrated D-Band Phased Arrays for 6G Wireless Communications** ***Mohamed Elkhouly*****,** *Bell Laboratories, New Providence, NJ*
10:45 AM	**Sub-Terahertz Transceivers in Silicon** ***Minoru Fujishima*****,** *Hiroshima University, Higashi-Hiroshima, Japan*
11:30 AM	**ICs and Transceiver Module Design for 100-300GHz Wireless** ***Mark J. W. Rodwell*****,** *University of California, Santa Barbara, CA*
12:15 PM	Lunch
1:30 PM	**Sub-THz InP-Based Wireless Connection Techniques Toward 6G** ***Hiroshi Hamada*****,** *NTT DoCoMo, Yokosuka, Japan*
2:15 PM	**Measurement and Validation of Sub-THz Radios: What Will it Take?** ***Roger Nichols*****,** *Keysight Technologies, Santa Rosa, CA*
3:00 PM	Break
3:15 PM	**Concepts, Architectures and Circuits for Sub-THz Sensing and Imaging** ***A. Stelzer*****,** *Linz University, Linz, Austria*
4:00 PM	Conclusion

F4: Paving the Way to 200Gb/s Transceivers

Organizers: ***Patrick Yue,*** *Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*
Sudip Shekhar, *University of British Columbia, Vancouver, Canada*

Committee: ***Thomas Toifl,*** *Cisco Systems, Thalwil, Switzerland*
Bo Zhang, *Broadcom, Irvine, CA*
Munehiko Nagatani, *NTT, Kanagawa, Japan*
Milin Zhang, *Tsinghua University, Beijing, China*

Champions: ***Franz Dielacher,*** *Infineon Technologies, Villach, Austria*
Bill Redman-White, *HiLight Semiconductor, Southampton, United Kingdom*

This Forum aims to provide a comprehensive background for the upcoming 200Gb/s electrical and optical links. Seven industry and academic experts will address the state of the art and offer insightful projections on related topics, including standards, circuits and technology. The Forum will begin with the design considerations for different standardizations of end-to-end channels at 224Gb/s. Next, the challenges and opportunities of serial transceiver design, signaling schemes beyond PAM4, equalization, DSP, and advanced forward-error-correction techniques will be presented. Switching gears to the technology side of things, the advancements in CMOS, semiconductor and silicon photonic technologies in supporting 200Gb/s operations will be discussed. A design example of a coherent optical transceiver will conclude the forum presentation.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Patrick Yue,*** *Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*
8:20 AM	**224 Gb/s Transceiver, End-to-End Channels, and Standardizations** ***Mike Li,*** *Intel, San Jose, CA*
9:05 AM	**200Gb/s Serial Transceiver Design: Challenges and Opportunities** ***Jonathan Rogers,*** *Alphawave IP, Toronto, Canada*
9:50 AM	Break
10:00 AM	**200Gb/s: Beyond PAM4** ***Gain Kim,*** *Samsung Electronics, Seoul, Korea*
10:45 AM	**DSP-Based Transceivers for 200Gb/s: Challenges and the Path Forward** ***Tamer Ali,*** *Mediatek, Irvine, CA*
11:30 AM	**Advanced FEC for 200Gb/s Transceiver Applications** ***Xinyuan Wang,*** *Huawei Technologies, Beijing, China*
12:15 PM	Lunch
1:30 PM	**Semiconductor Technology – the Path Forward for the Coming Decades** ***Philip Wong,*** *Stanford, Palo Alto, CA*
2:15 PM	**Silicon Photonics Technology for Next-Generation Transceivers** ***Joris Van Campenhout,*** *IMEC, Leuven, Belgium*
3:00 PM	Break
3:15 PM	**Coherent Optical Transceivers for >200Gb/s per Wavelength** ***Alex Rylyakov,*** *Nokia, New York, NY*
4:00 PM	Conclusion

F5: How to Improve AI Efficiency Further: New Devices, Architectures and Algorithms

Organizers: ***Rangharajan Venkatesan,*** *NVIDIA, Santa Clara, CA*
Alicia Klinefelter, *NVIDIA, Durham, NC*

Committee: ***Kea-Tiong Tang,*** *National Tsing Hua University, Hsinchu, Taiwan*
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Mingoo Seok, *Columbia University, New York, NY*
Shidhartha Das, *Arm, Cambridge, United Kingdom*

Champions: ***Yan Li,*** *Western Digital, Milpitas, CA*
Fatih Hamzaoglu, *Intel, Hillsboro, OR*

Machine learning (ML) algorithms and applications continue to evolve at a rapid pace relative to Moore's Law. There is simultaneously a demand for bigger and more complex ML models, ever-growing computational throughput and improved energy efficiency over the coming decade. As we start to hit the limits of technology scaling, what are the latest design strategies to improve performance and energy efficiency of machine learning processors of the future? Further, can ML-based tools improve hardware design methodology? This forum aims to explore novel circuits, architectures, algorithms, as well as ML-based chip design tools that will push the limits of AI efficiency.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Rangharajan Venkatesan,*** *NVIDIA, Santa Clara, CA*
8:20 AM	**GPU Architectures for Efficient Deep Learning** ***Ronny Krashinksy*****,** *NVIDIA, Santa Clara, CA*
9:05 AM	**Mixed-Signal Compute-in-Memory Processing for Energy Efficient Algorithms** ***Laura Fick*****,** *Mythic, Cedar Park, TX*
9:50 AM	Break
10:00 AM	**Neuromorphic Intelligence: Using Populations of Inhomogeneous Spiking Neurons to Carry Out Robust Computation in Neuromorphic Processors** ***Giacomo Indiveri*****,** *University of Zurich and ETH Zurich, Zurich, Switzerland*
10:45 AM	**Artificial Intelligence Processor Using Photonic Computing** ***Xing Lin*****,** *Tsinghua University, Beijing, China*
11:30 AM	**Quantization Techniques for Low-Precision Inference and Training** ***Kailash Gopalakrishnan*****,** *IBM Research, Yorktown Heights, NY*
12:15 PM	Lunch
1:30 PM	**Graphs: Powerful But Hard to Beat** ***Stijn Eyerman*****,** *Intel, Kontich, Belgium*
2:15 PM	**Acceleration for Graph Neural Network Inference** ***Sachin S. Sapatnekar*****,** *University of Minnesota, Minneapolis, MN*
3:00 PM	Break
3:15 PM	**Machine Learning in Chip Design Tools** ***Evangeline Young*****,** *Chinese University of Hong Kong, Shatin, Hong Kong*
4:00 PM	Conclusion

F6: Computer Systems Under Attack – Paying the Performance Price for Protection

Organizer: ***Massimo Alioto,*** *National University of Singapore, Singapore*

Committee: ***Ingrid Verbauwhede,*** *KU Leuven, ESAT-COSIC, Leuven, Belgium*
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Dong Uk Lee, *SK hynix, Icheon-si, Korea*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*

Champion: ***Vivek De,*** *Intel, Hillsboro, OR*

Present-day computer systems are increasingly under attack on multiple fronts with new vulnerabilities being discovered every day at system, architecture, memory and physical level. While countermeasures against such attacks exist, they often impose significant overheads in performance and power. This forum will give an overview of recent security vulnerabilities, including speculative side-channels, memory exploits, physical attacks and discuss the overheads of detecting/mitigating against them. The forum also includes post-quantum cryptographic algorithms and homomorphic encryption accelerators that promise very high security value propositions, while imposing orders-of-magnitude increase in computational complexity.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** ***Massimo Alioto,*** *National University of Singapore, Singapore*
8:20 AM	**Overview of Security Challenges, Applications, Common Practice and Directions in SOC Design** ***Serge Leef,*** *Darpa, Bellevue, WA*
9:05 AM	**Microarchitectural Side-Channel Attacks** ***Todd Austin,*** *University of Michigan, Ann Arbor, MI*
9:50 AM	Break
10:00 AM	**Microarchitectural Vulnerabilities: Evolving Landscape** ***Carlos Rozas,*** *Intel, Portland, OR*
10:45 AM	**DRAM Circuit Design for Protecting Natural/Artificial Faults and Reliability Degradation** ***Dongkyun Kim,*** *SK hynix, Icheon-si, Korea*
11:30 AM	**Memory Architecture Mitigations and Impact on System-Level Performance** ***Ruby Lee,*** *Princeton University, Princeton, NJ*
12:15 PM	Lunch
1:30 PM	**Physical Side-Channel Attacks and Counteraction Through Design Automation** ***Ileana Buhan,*** *Radboud University, Nijmegen, the Netherlands*
2:15 PM	**Integrated Sense-and-React Countermeasures Against Physical Attacks** ***Noriyuki Miura,*** *Osaka University, Osaka, Japan*
3:00 PM	Break
3:15 PM	**Hardware Implementation Challenges in Post-Quantum Encryption and Fully Homomorphic Encryption** ***Sujoy Sinha Roy,*** *Graz University of Technology, Graz, Austria*
4:00 PM	Conclusion

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Tuesday, February 22:	**8:00 am to 3:00 pm**
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Thursday, February 24:	**7:00 am to 2:00 pm**

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Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 9, 2022.** After January 9th, and before 12:00 Midnight EST **Sunday January 23, 2022,** registrations will be processed **at the Late Registration rates. After January 26th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

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No refunds will be made after 12:00 Midnight EST January 23, 2022. Paid registrants who do not attend the conference will be sent all relevant conference materials.

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Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/abouUhelp/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

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Get Connected! Stay Current! Invest in your Career! Membership in the Solid-State Circuits Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

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-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

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SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.
University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.
Publications: Conference registration includes:
-The **Digest of Technical Papers** on USB. This year, as part of your Conference registration, the e Digest of Technical Papers will be provided on a USB, as well as part of the download. The e-Digest will include all 3 pages for each paper. Note that all 3 pages for each paper will be available on IEEE Xplore.
-Papers Visuals: The visuals from all papers presented will be available by download.
-Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be availableby download.
-Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are twelve 90-minute Tutorials that will be available virtually, not in person at the conference. The forums and Short Course will be live, in-person. There will be two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

OPTIONAL PUBLICATIONS

ISSCC 2022 Publications: The following ISSCC 2022 digital publications can be purchased in advance or on site:
2022 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in June)**
2022 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**
2022 Short Course USB: High Speed/High Performance Data Converters: Metrics, Architectures, and Emerging Topics **(mailed in June).**
The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.
Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:
-Items listed on the registration website can be purchased with registration and picked up at the conference.
-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materialsat this desk. See the posted list at the Conference for titles and prices.
-Visit the ISSCC website at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $285 for a single/double** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free.** All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2022 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 29, 2022 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 29th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmationnumber ready.

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EVENT PHOTOGRAPHY

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REFERENCE INFORMATION

Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Registration questions:	ISSCCinfo@yesevents.com	
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com	Phone: 416-418-3034
Registration:	YesEvents PO Box 3024 Westminster, MD 21158 Email: issccinfo@yesevents.com	Phone: 800-937-8728 Fax: 410-559-2236

Hotel Transportation: Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at
www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

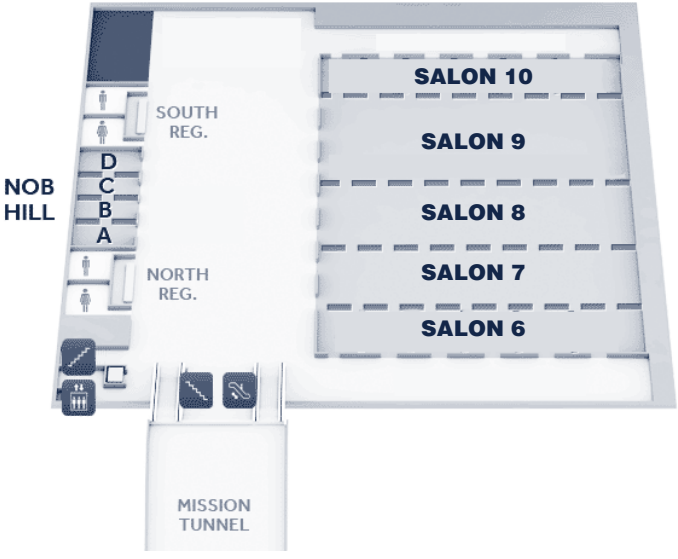
Next ISSCC Dates and Location:
ISSCC 2023 will be held on February 19 - 23, 2023
at the San Francisco Marriott Marquis Hotel.

SUBCOMMITTEE CHAIRS

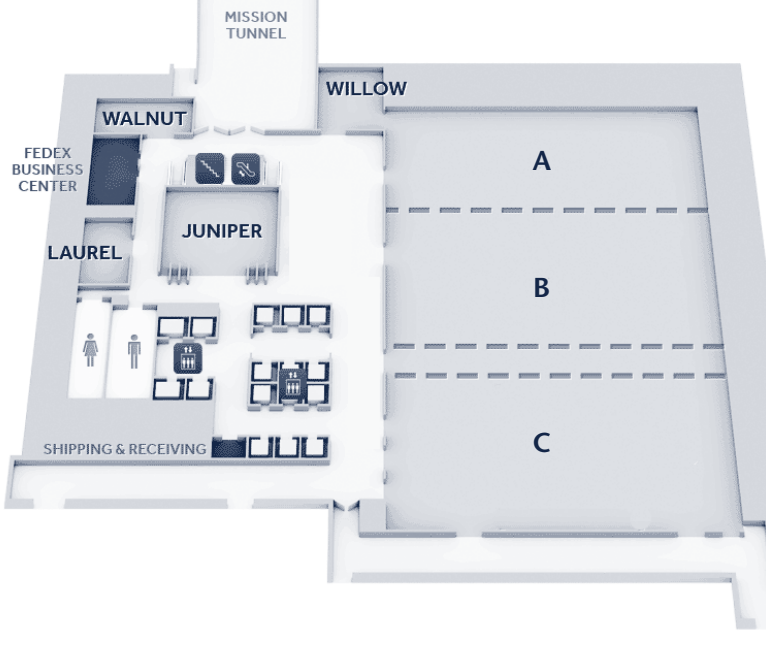
Analog:	Maurits Ortmanns
Data Converters:	Michael Flynn
Digital Architectures & Systems:	Thomas Burd
Digital Circuits:	Keith Bowman
Imagers, MEMS, Medical & Displays:	Chris van Hoof
Machine Learning & AI	Marian Verhelst
Memory:	Meng-Fan Chang
Power Management:	Yogesh K. Ramadass
RF:	Jan Craninckx
Technology Directions:	Makoto Nagata
Wireless:	Stefano Pellerano
Wireline:	Yohan Frans

Program-Committee Chair:	Edith Beigné
Program-Committee Vice-Chair:	Piet Wambacq
Conference Chair:	Kevin Zhang

Lower B2 Level - Yerba Buena Ballroom



B2 Level - Golden Gate Hall



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